Title	**150 W Three-Phase Inverter Using BridgeSwitch™-2 BRD2463C and LinkSwitch™-TN2 LNK3205D in FOC Operation**
Specification	340 VDC Input, 150 W Continuous Three-Phase Inverter Output Power, 750 mA_{RMS} Continuous Motor Phase Current
Application	High-Voltage Brushless DC (BLDC) Motor Drive
Author	Applications Engineering Department
Document No.	RDR-974
Date	November 19, 2024
Revision	C

Summary and Features

- BridgeSwitch-2 – high-voltage half-bridge motor driver
- Integrated 600 V FREDFETs with ultra-soft, fast recovery diodes
- No heat sink
- Fully self-biased operation – simplifies auxiliary power supply but can also support external bias operation as needed
- High-side and low-side cycle-by-cycle current limit
- Optional latching low-side current limit
- Configurable latching or hysteretic over-temperature protection
- High-voltage bus monitor for overvoltage protection
- Simplified error flagging through the Error Flag (EF) pin on the interface
- Supports any microcontroller (MCU) for sensorless field-oriented control (FOC) through the signal interface
- Instantaneous phase current output signal for each BridgeSwitch-2 device
- +5 V supply available through the interface
- Less than 10 mW inverter no-load power consumption using Sleep Mode

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Important Note:
During operation, the reference design board is subject to hazards including high voltages, rotating parts, bare wires, and hot surfaces. Energized DC bus capacitors require time to discharge after DC input disconnection.

All testing should use an isolation transformer to provide the DC input to the board.

1 Introduction

This document describes a 150 W, 96% efficient, three-phase inverter for high-voltage brushless DC (BLDC) motor application with three BridgeSwitch-2 BRD2463C devices. The design shows the device performance, internal level monitoring, system level monitoring, and fault protection facilitated by the high level of integration of the BridgeSwitch-2 half-bridge motor driver IC. A high-voltage, low component count buck converter using the LinkSwitch-TN2 LNK3205D device supplies the current sense amplifier and optionally provides external bias for the BridgeSwitch-2 devices.

Also included in this report are the inverter specifications, schematic, bill of materials, printed circuit board (PCB) layout, performance data, and test setup. The provided waveforms and performance data are based on a sensorless field-oriented control (FOC) method employing the Space Vector Modulation (SVM) scheme commonly referred to as three-phase modulation in this document. This is implemented by the MotorXpert Suite by using the instantaneous phase current (IPH) information as current feedback.

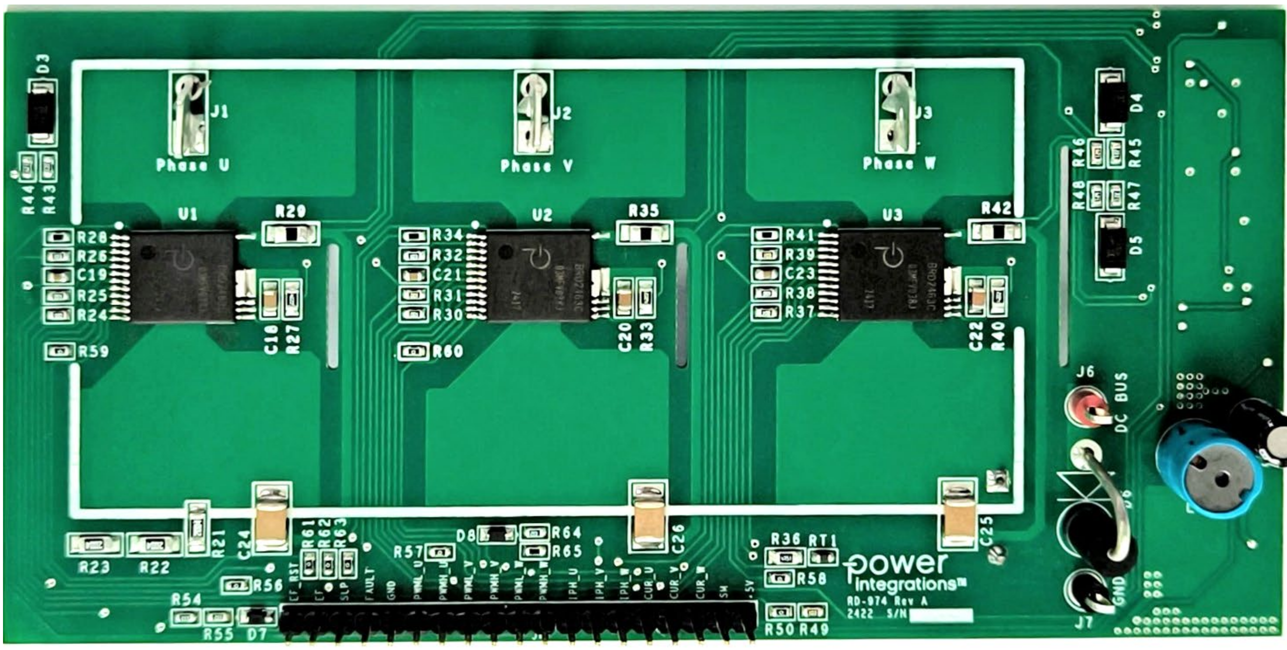

Figure 1 – Populated Circuit Board Top View.

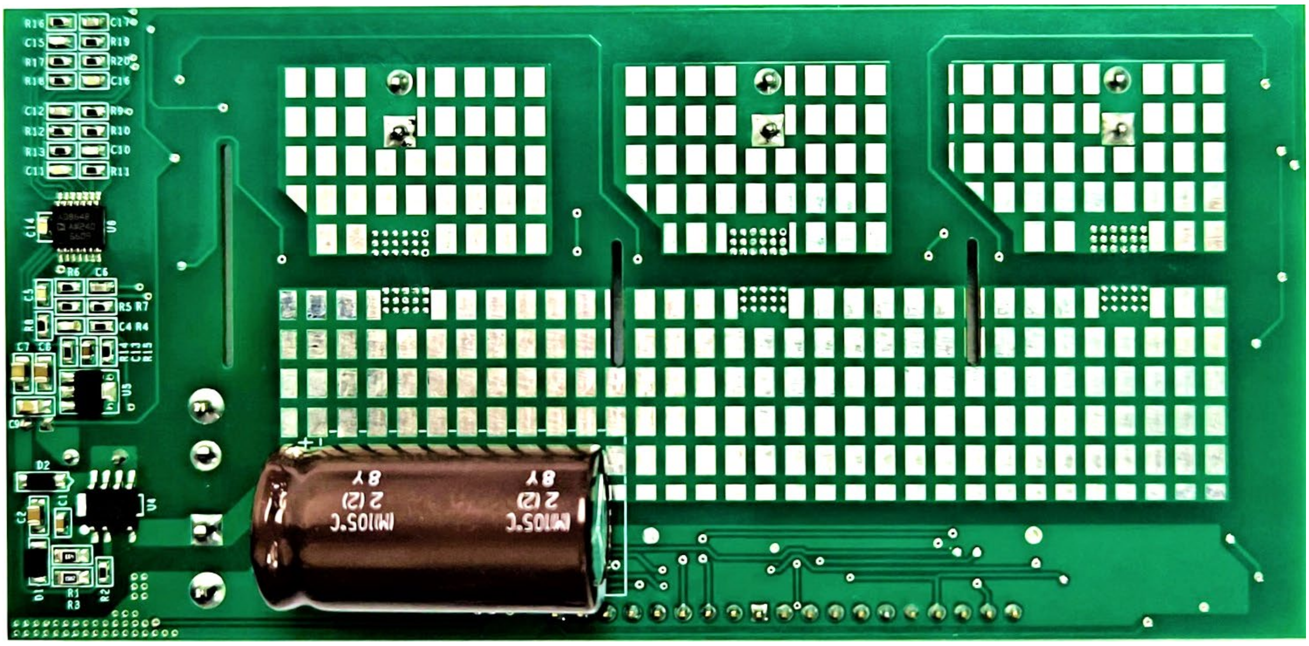

Figure 2 – Populated Circuit Board Bottom View.

2 Inverter Specification

The table below summarizes the electrical specifications and performance data of the three-phase inverter design.

Description	Symbol	Min	Typ	Max	Unit	Comment
Input						
Voltage	V_{IN}	270	340	365	V	2-wire DC Input.
Current	I_{IN}		0.46		A_{RMS}	RMS.
Power	P_{IN}		153		W	At Efficiency = 96%.
Output						
Power	P_{OUT}		147		W	Inverter Output Power.
Motor Phase Current	$I_{MOT(RMS)}$		0.75		A_{RMS}	Continuous RMS per Phase.
Inverter Peak Output Current	$I_{INT(PK)}$		2.50		A	Inverter Peak Current.
PWM Carrier Frequency[1]	f_{PWM}		10		kHz	Three-Phase FOC Modulation.
Inverter Efficiency	η		96		%	Self-Supplied Operation.
Output Speed	ω		3000		RPM	Motor Speed at 150 W Inverter Output.
Environmental						
Ambient Temperature	T_{AMB}	-20	29	65	°C	Average Ambient Temperature. Closed-case. Free Convection.
Device Case Temperature	$T_{PACKAGE}$		75	111	°C	0.75 A_{RMS} Phase Current in Self-Supplied Operation.
System Level Monitoring						Reported through the Error Flag (EF) Pin.
DC Bus Sensing						
OV Threshold	V_{OV}		362		V	
Over Current Protection[2]	I_{OCP}		2.50		A_{PK}	At XL/XH = 42.2 kΩ

Notes:
1. 20 kHz is the maximum recommended PWM frequency with self-supply
2. This can be manually configured by adjusting the value of the XL/XH resistors. For BRD2463C, the maximum current protection level is 2.50 A at an XL/XH resistance of 42.2 kΩ.

Table 1 – Inverter Specification.

3 Schematic

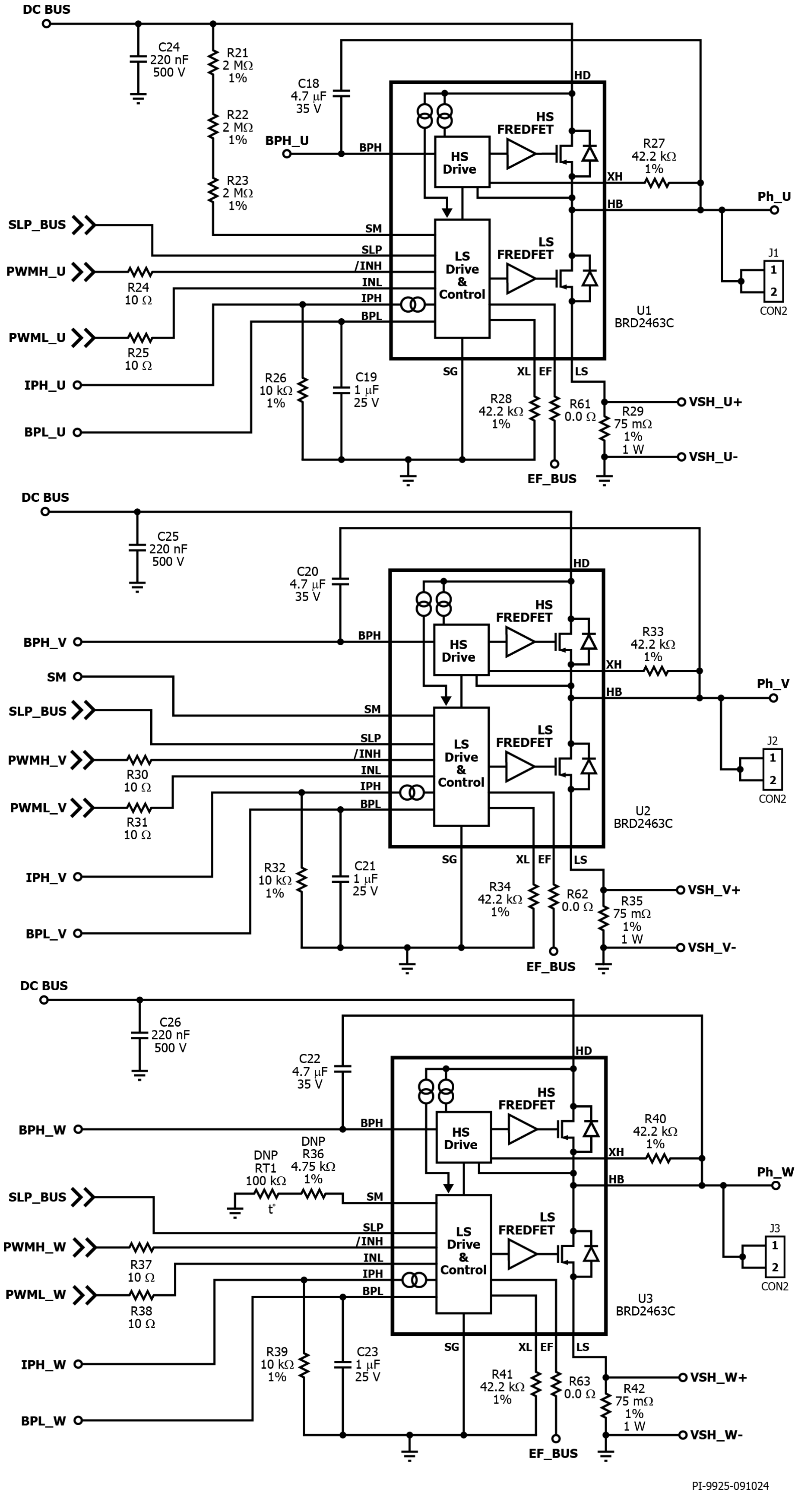

Figure 3 – BridgeSwitch Three-Phase Inverter Schematic.

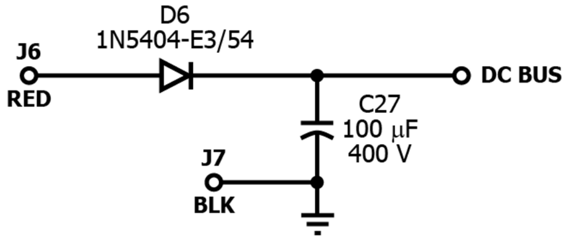

Figure 4 – Input Stage Schematic.

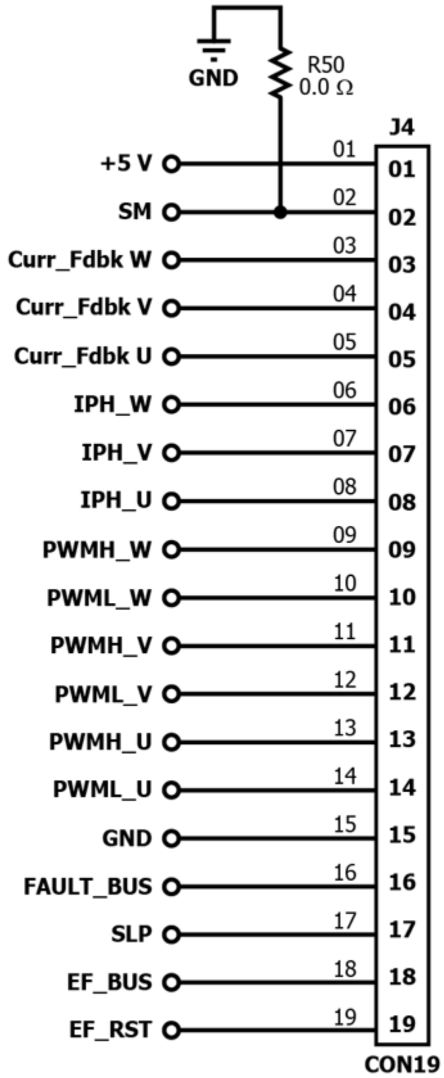

Figure 5 – Microcontroller Interface Schematic.

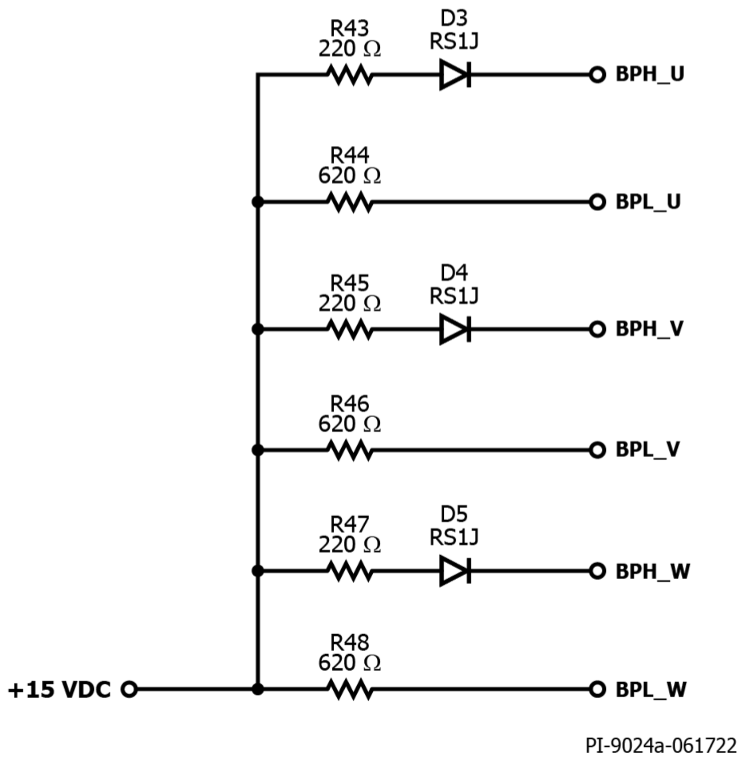

Figure 6 – External Supply Components Schematic.

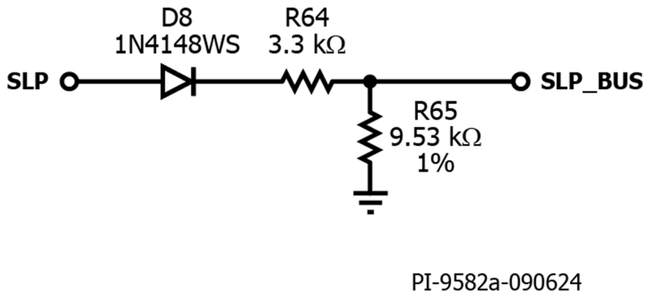

Figure 7 – Sleep Mode Circuit Schematic.

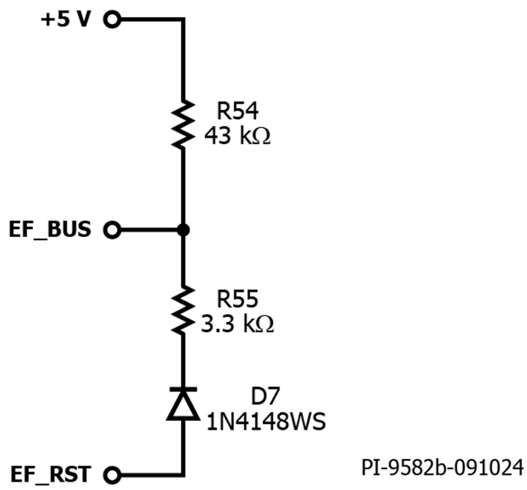

Figure 8 – Error Flag Circuit Schematic.

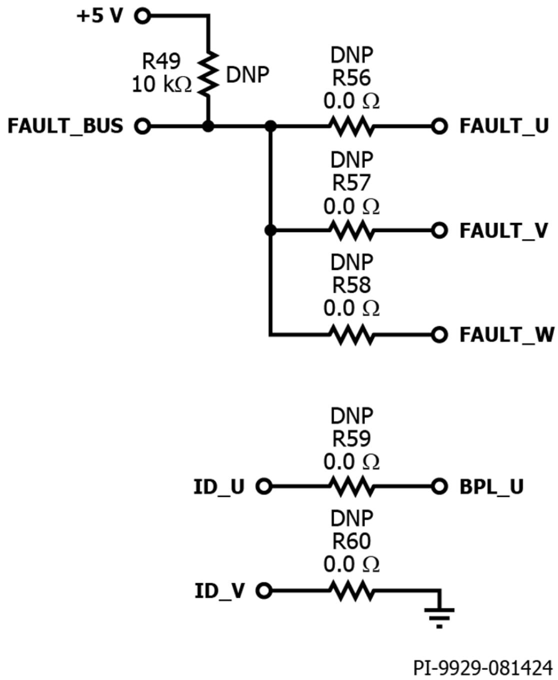

Figure 9 – FAULT Bus and Device ID Components Schematic.

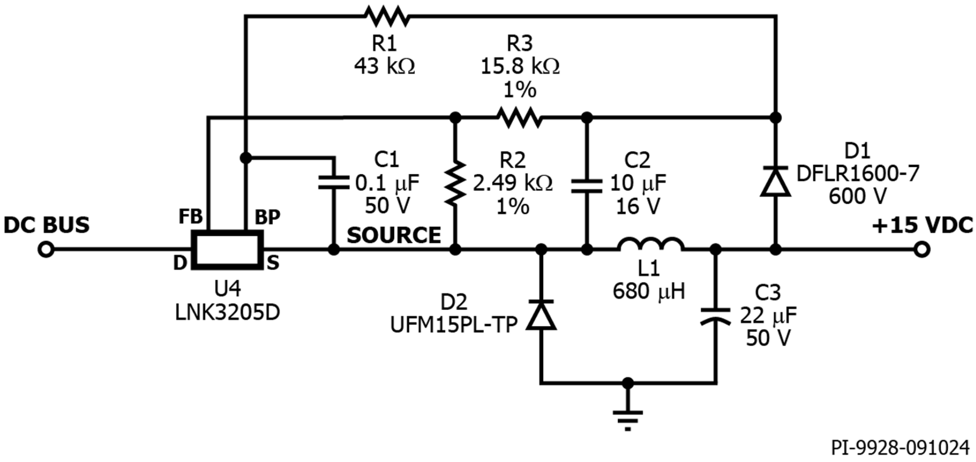

Figure 10 – 15 V Auxiliary Supply Schematic.

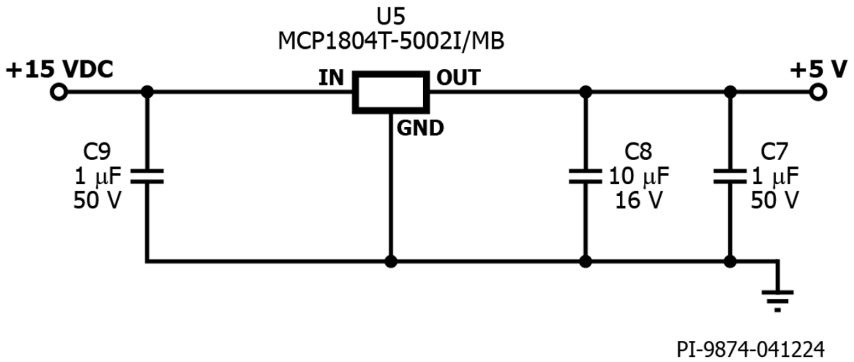

Figure 11 – 5 V Linear Regulator Circuit Schematic.

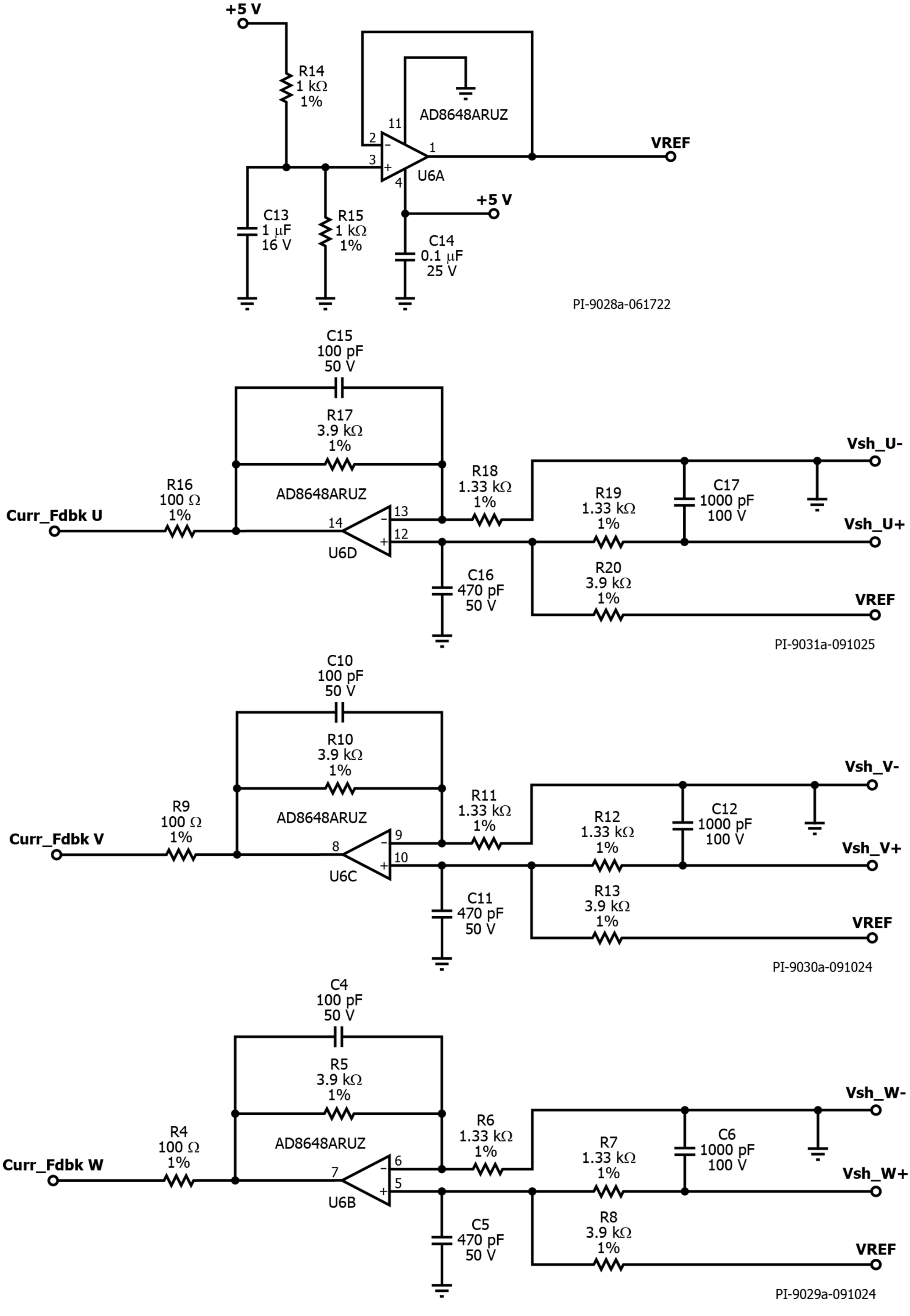

Figure 12 – Current Sense Amplifier Circuit Schematic.

4 Circuit Description

This reference design features a three-phase inverter with three BridgeSwitch-2 BRD2463C devices to drive a high-voltage, three-phase, brushless DC (BLDC) motor implementing field-oriented control (FOC). Each BridgeSwitch-2 device combines two 600 V, N-channel power FREDFETs with their corresponding gate drivers into a low-profile surface mount package. The power FREDFET features an ultra-soft, fast-recovery diode ideally suited for inverter drives. Both low-side and high-side gate drivers are fully self-supplied eliminating the need for an additional power supply to provide gate drive power.

A LinkSwitch-TN2 LNK3205D device in a high-voltage buck converter provides an optional 15 V supply for the BridgeSwitch-2 in the external bias configuration and serves as input to the 5 V linear regulator powering up the current sense amplifier circuit.

Additionally, the BridgeSwitch-2 device incorporates internal fault protection which includes cycle-by-cycle current limit for both FREDFETs, thermal overload protection, and high-voltage DC bus sensing to protect against overvoltage conditions. A single-wire bus inhibits device switching and communicates with the system microcontroller during these detected faults.

4.1 Three-Phase BridgeSwitch Inverter

The BridgeSwitch-2 devices U1, U2, and U3 form the three-phase inverter. The output of the inverter connects to the three-phase BLDC motor through connectors J1, J2, and J3.

4.2 Input Stage

The input stage consists of terminals J6 and J7, input diode D6, and bulk capacitor C27. Terminals J6 (positive) and J7 (negative) serve as connectors for the high-voltage DC bus. The bulk capacitor C27 minimizes the path from the high-voltage DC supply to the board and stabilizes the DC bus. Input diode D6 protects the bulk capacitor from reversed DC voltage and prevents load current from flowing back to the source during abnormal operating conditions.

4.3 BridgeSwitch Bias Supply

Capacitors C19, C21, and C23 provide self-supply decoupling for the integrated low-side controller and gate driver. An internal high-voltage current source charges these capacitors upon reaching the minimum bus voltage.

On the other hand, capacitors C18, C20, and C22 provide self-supply decoupling for the integrated high-side controller and gate driver. An internal high-voltage current source charges these capacitors whenever the low-side FREDFET turns on, completing the path from the half-bridge point to the power ground.

4.4 PWM Input

Input PWM signals PWML_U, PWMH_U, PWML_V, PWMH_V, PWML_W, PWMH_W control the switching states of the integrated high-side and low-side power FREDFETs. The system microcontroller provides the PWM signal at the desired switching frequency. Resistors R24, R25, R30, R31, R37, and R38 serve as PWM signal filters before connecting to the INL and /INH pins of the BridgeSwitch-2 device.

4.5 Error Flag

The BridgeSwitch-2 (BRD2463C) features the new error flag pin which simplifies fault communication with the microcontroller. It is pulled up to 5 V by resistor R54 and connects to a single bus through resistors R61, R62, and R63.

During latching conditions, such as after latching overcurrent and over-temperature protection faults, the EF pin is automatically pulled down to inhibit FREDFET switching until either a power recycle, or an EF reset signal through components D7 and R55. No action is required for resetting the EF pin after hysteretic protection conditions such as overvoltage and hysteretic over-temperature states.

4.6 Cycle-by-Cycle Current Limit

Resistors R28, R34, R41, R27, R33, and R40 set the cycle-by-cycle current limit level for the integrated low-side and high-side power FREDFETs. A selected value of 42.2 kΩ sets the current limit to 100% of the default level (2.50 A_{PK}). The cycle-by-cycle overcurrent protection for the low-side FREDFET is selected by setting the SLP programming resistor R65 to either 9.53 kΩ or OPEN (≥1 MΩ). This is the default setting for this reference design.

4.7 Latching Current Limit

Setting the SLP programming resistor R65 to 133 kΩ activates the latching current limit protection for the low-side power FREDFET. In this configuration, the low-side FREDFET latches off after a sustained overcurrent state over sixteen consecutive switching cycles. The Error Flag pin is pulled down to inhibit switching and is only pulled up after receiving an EF reset signal or a power recycle.

4.8 Overvoltage (OV) Protection

The BridgeSwitch-2 device (U1) monitors the DC bus voltage through resistors R21, R22, and R23 with a combined resistance of 6 MΩ. This sets the bus overvoltage threshold at 362 VDC. The Error Flag pin is pulled down to inhibit FREDFET switching when the bus voltage exceeds this threshold and is automatically pulled up once the bus voltage drops below the hysteresis level.

4.9 FAULT Bus Provisions

BridgeSwitch-2 devices U1, U2, and U3 may also be populated with BRD2263C devices if the FAULT bus functionality is desired. The fault pins connect to a single fault bus through resistors R56, R57, and R58, and pulled-up to 5 V by R49. The FAULT bus reports any detected internal and system status change through pin 16 of connector J4.

4.10 Device ID Provisions

For FAULT bus applications, each BridgeSwitch-2 device assigns itself a unique device ID by altering the pin 11 (ID) connection. This pin can be floating, connected to the SG pin through R60, or connected to the BPL pin through R59. The device ID allows the specific device flagging a fault to communicate its physical location to the system microcontroller.

4.11 System Undervoltage Status Updates

The FAULT Bus enables fault flagging during undervoltage conditions. This is set through resistors R21, R22, and R23, the same components for determining the overvoltage protection threshold. A 6 MΩ combined resistance sets the undervoltage thresholds to 212 V, 182 V, 152 V, and 122 V.

4.12 System Monitoring Provisions

System temperature monitoring is possible with the FAULT Bus through thermistor RT1 connected to the SM pin (U3). Resistor R36 tunes the threshold to the desired level for a system thermal fault flag reported by the FAULT pin. Alternatively, an external sensor may be connected to the SM pin (U2) through pin 2 of connector J4 after depopulating resistor R50.

4.13 Sleep Mode

The new sleep mode is designed to reduce the standby input power consumption by disabling the low-side driver functionality during non-operation. It is enabled by setting the SLP Bus HIGH (min. 2.5 V) through components D8 and R64.

4.14 Microcontroller (MCU) Interface

Connector J4 allows the system microcontroller to interface with the BridgeSwitch-2 three-phase inverter. It provides access to the following signals:

- **EF_RST –** Input pin for the EF reset signal (for releasing latching conditions)
- **EF** – Bi-directional pin for Error Flag state monitoring and inhibiting FREDFET switching
- **SLP –** Input pin for the sleep mode enable signal
- **GND** – Common ground interface between the microcontroller and the inverter board
- **PWMH_U, PWML_U, PWMH_V, PWML_V, PWMH_W, and PWML_W** – Input pins for the low-side and high-side FREDFET PWM control signals
- **+5 V** – Voltage supply pin for the microcontroller as needed
- **SM** – Configurable system monitoring pin for the BridgeSwitch device (U2).
- **Curr_fdbkU, Curr_fdbkV, Curr_fdbkW** – Current feedback information from the inverter shunt resistors processed by the signal conditioning circuit
- **IPH_U, IPH_V, IPH_W** – Low-side FREDFET instantaneous phase current information from the IPH pin

4.15 External Supply

Components R43, R44, R45, R46, R47, R48 and diodes D3, D4, and D5 are responsible for providing external supply to the BridgeSwitch BPL and BPH pin through device U4. External supply operation is optional for applications that require higher efficiency or operate at elevated ambient temperatures. Otherwise, these components can be depopulated and the BPL and BPH supplies will be drawn internally from the BridgeSwitch-2 device (self-supply mode).

4.16 Auxiliary Power Supply Circuit

Device U4 (LNK3205D) is a high-side buck switcher IC responsible for providing optional 15 V supply to the BPL and BPH pins, and input to the 5 V linear regulator. It steps down the high-voltage DC input to a lower output voltage.

For more information about LNK3205D, please refer to the datasheet through the following link: https://ac-dc.power.com/design-support/product-documents/data-sheets/linkswitch-tn2-data-sheet/

4.17 5 V Output Linear Regulator

Device U5 (MCP1804T) is a 5 V linear regulator that supplies the signal conditioning circuit, and the microcontroller through pin 1 of connector J4.

4.18 Current Sense Amplifier

Components U6B, U6C, and U6D are current sense amplifiers which process current information from shunt resistors R29, R35, and R42. A 2.5 VDC offset is provided by the U6A circuit to maintain the shunt resistor signals within the positive range. The microcontroller receives the U6B, U6C, and U6D circuit outputs to use as current feedback for implementing the desired motor control algorithm.

Note: U6A, U6B, U6C, and U6D are op-amps in one IC package (Quad op-amp, U6)

5 Printed Circuit Board Layout

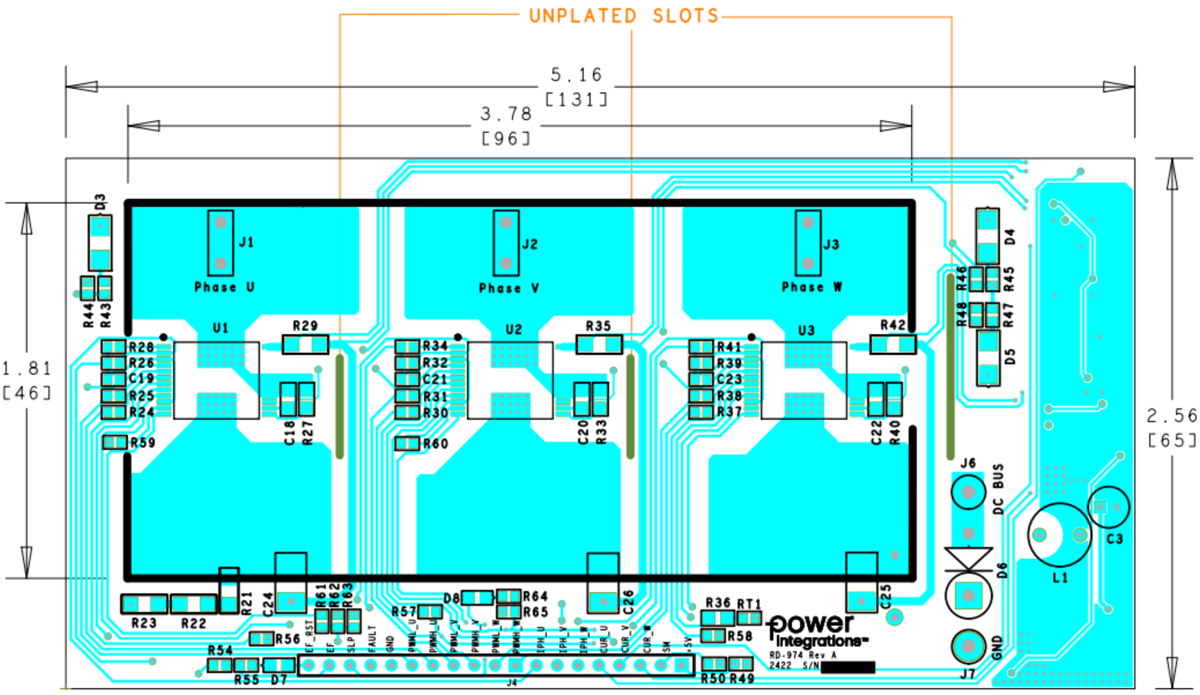

Figure 13 – Printed Circuit Board Layout Top View.

Note:

1. The overall PCB dimension is 131 mm x 65 mm (L x W).
2. The inverter PCB dimension is 96 mm x 46 mm (L x W) – in black rectangle.
3. PCB Specifications:
   - Board thickness: 0.062 inches
   - Board material: FR4
   - Copper weight: 2 oz
   - No. of layers: 2

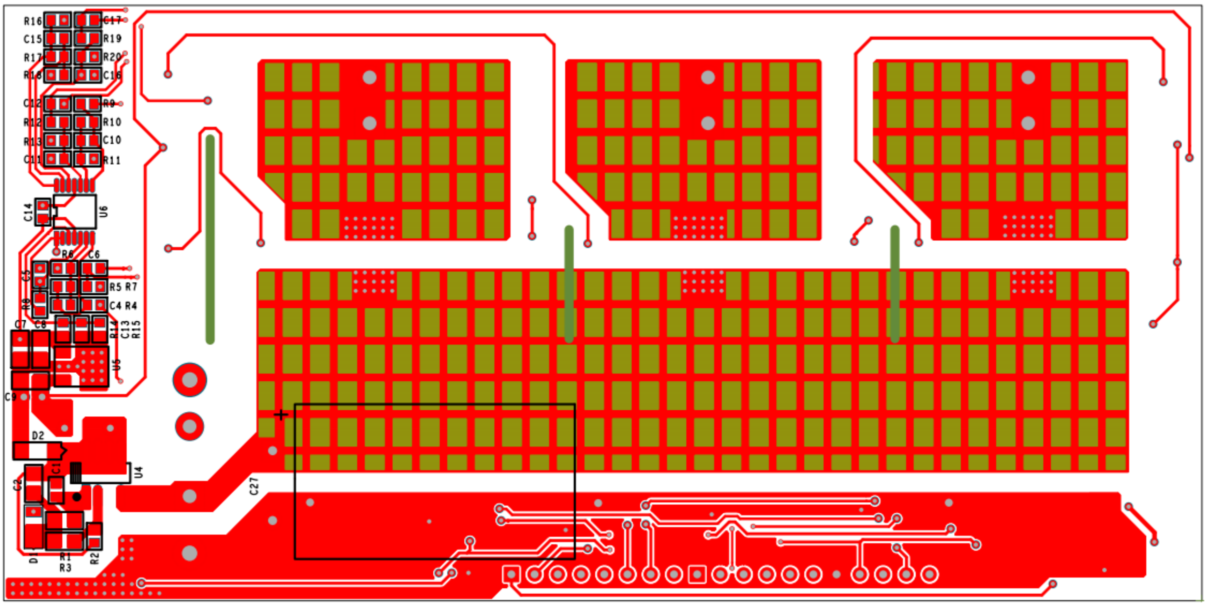

Figure 14 – Printed Circuit Board Layout Bottom View.

6 Bill of Materials

Item	Qty	Ref Des	Description	Mfg Part Number	Mfg
1	1	C1	0.1µF ±10%, 50V, Ceramic, X7R, 0603	CGA3E2X7R1H104K080AA	TDK
2	2	C2, C8	10 µF, ±10%, 16V, X7R, Ceramic, SMT, MLCC 0805	CL21B106KOQNNNE	Samsung
3	1	C3	22 µF, 50 V, Electrolytic, (5 x 11)	UPW1H220MDD	Nichicon
4	3	C4, C10, C15	100 pF, 50 V, Ceramic, NP0, 0603	CC0603JRNPO9BN101	Yageo
5	3	C5, C11, C16	470 pF, 50 V, Ceramic, C0G/NP0, 0603	VJ0603A471JXAAC	Vishay
6	3	C6, C12, C17	1000 pF, 100 V, Ceramic, NP0, 0603	C1608C0G2A102J	TDK
7	2	C7, C9	1 µF, 50 V, Ceramic, X5R, 0805	08055D105KAT2A	AVX
8	1	C13	1 µF, 16 V, Ceramic, X7R, 0603	CL10B105KO8VPNC	Samsung
9	1	C14	100 nF, 25 V, Ceramic, X7R, 0603	VJ0603Y104KXXAC	Vishay
10	3	C18, C20, C22	4.7 µF, ±10%, 35V, Ceramic, X7R, 0805	C2012X7R1V475K125AE	TDK
11	3	C19, C21, C23	1 µf, ±10%, 25 V, Ceramic, X7R, 0603	CGA3E1X7R1E105K080AE	TDK
12	3	C24, C25, C26	220 nF, 500 V, Ceramic, X7R, 1812	C1812C224KCRACTU	Kemet
13	1	C27	100 µF, 400 V, Electrolytic, Low ESR, (16 x 30)	EPAG401ELL101ML30S	Nippon Chemi-Con
14	1	D1	600 V, 1 A, Rectifier, Glass Passivated, POWERDI123	DFLR1600-7	Diodes, Inc.
15	1	D2	600 V, 1 A, Ultrafast Recovery, 75 ns, SOD-123	UFM15PL-TP	Micro Commercial
16	3	D3, D4, D5	600 V, 1 A, Fast Recovery, 250 ns, SMA	RS1J-13-F	Diodes, Inc.
17	1	D6	400 V, 3 A, Rectifier, DO-201AD	1N5404-E3/54	Vishay
18	2	D7, D8	General Purpose, 75 V, 150 mA, SOD-323	1N4148WS-7-F	Diodes, Inc.
19	3	J1, J2, J3	0.250" Quick Connect Male	1287-ST	KeyStone
20	1	J4	(1 x 19) Male header, 0.1 pitch, Vertical, Au	PH1-19-UA	Adam Tech
22	1	J6	Test Point, RED, Thru-hole Mount	5010	Keystone
23	1	J7	Test Point, BLK, Thru-hole Mount	5011	Keystone
24	1	L1	680 µH, 0.36 A	SBC3-681-361	SUNX
25	1	R1	RES, 43 kΩ, 5%, 1/8 W, Thick Film, 0805	ERJ-6GEYJ433V	Panasonic
26	1	R2	RES, 2.49 kΩ, 1%, 1/10 W, Thick Film, 0603	ERJ-3EKF2491V	Panasonic
27	1	R3	RES, 15.8 kΩ, 1%, 1/8 W, Thick Film, 0805	ERJ-6ENF1582V	Panasonic
28	3	R4, R9, R16	RES, 100 Ω, 1%, 1/10 W, Thick Film, 0603	ERJ-3EKF1000V	Panasonic
29	6	R5, R8, R10, R13, R17, R20	RES, 3.9 kΩ, ±1%, 0.1W, 1/10W, 0603, Automotive, AEC-Q200, Thick Film	ERJ-3EKF3901V	Panasonic
30	6	R6, R7, R11, R12, R18, R19	RES, 1.33 kΩ, 1%, 1/10 W, Thick Film, 0603	ERJ-3EKF1331V	Panasonic
31	2	R14, R15	RES, 1 kΩ, 1%, 1/10 W, Thick Film, 0603	ERJ-3EKF1001V	Panasonic
32	2	R21, R22, R23	RES, 2 MΩ, 1%, 1/4 W, Thick Film, 1206	ERJ-8ENF2004V	Panasonic
33	6	R24, R25, R30, R31, R37, R38	RES, 10 Ω, 5%, 1/10 W, Thick Film, 0603	ERJ-3GEYJ100V	Panasonic
34	3	R26, R32, R39	RES, 10 kΩ, 1%, 1/10 W, Thick Film, 0603	ERJ-3EKF1002V	Panasonic
35	3	R27, R33, R40	RES, 42.2 kΩ, 1%, 1/8 W, Thick Film, 0805	ERJ-6ENF4222V	Panasonic
36	3	R28, R34, R41	RES, 42.2 kΩ, 1%, 1/10 W, Thick Film, 0603	ERJ-3EKF4222V	Panasonic
37	3	R29, R35, R42	RES, 75 mΩ, ±1%, 1W Chip Resistor, 1206, Automotive, AEC-Q200, Thick Film	ERJ-8BWFR075V	Panasonic
38	3	R43, R45, R47	RES, 220 Ω, 5%, 1/10 W, Thick Film, 0603	ERJ-3GEYJ221V	Panasonic
39	3	R44, R46, R48	RES, 620 Ω, 5%, 1/10 W, Thick Film, 0603	ERJ-3GEYJ621V	Panasonic
40	4	R50, R61, R62, R63	RES, 0 Ω, 5%, 1/10 W, Thick Film, 0603	ERJ-3GEY0R00V	Panasonic
41	1	R54	RES, 43 kΩ, 5%, 1/10 W, Thick Film, 0603	ERJ-3GEYJ433V	Panasonic
42	2	R55, R64	RES, 3.3 kΩ, 5%, 1/10 W, Thick Film, 0603	ERJ-3GEYJ332V	Panasonic
43	1	R65	RES, 9.53 kΩ, 1%, 1/10 W, Thick Film, 0603	ERJ-3EKF9531V	Panasonic
46	3	U1, U2, U3	BridgeSwitch-2, Max. BLDC Motor Current 3 A (DC), InSOP-24C	BRD2463C	Power Integrations
47	1	U4	LinkSwitch-TN2, SO-8C	LNK3205D	Power Integrations
48	1	U5	IC, REG, LDO, 5.0 V, 0.15 A, 28 Vin max, TO-243AA, SOT-89-3	MCP1804T-5002I/MB	MicroChip
49	1	U6	IC, GP Op-Amp, Quad, R2R, 14-TSSOP	AD8648ARUZ-REEL	Analog Devices

Table 2 – Bill of Materials.

7 Performance Data

This section includes waveforms and performance data of the BridgeSwitch-2 inverter. These were measured with a DC bus level of 340 VDC, and a 10 kHz PWM signal implementing the three-phase modulated field-oriented control at an ambient of 29 °C.

7.1 Start-Up Operation

7.1.1 Bypass Voltages Start-Up Waveforms

The waveforms below show the low-side and high-side bypass pin voltages in self-supply mode after a bus voltage of 340 VDC is applied. This follows the recommended start-up sequence described in Section 8.2 of the Appendix. For this measurement, the DC bus turn-on slew rate was set to 100 V/ms.

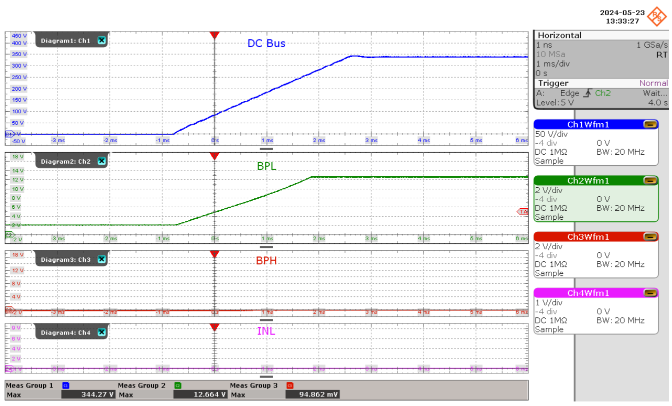

Figure 15 – BPL and BPH Signals at Start-up, INL LOW.
CH1: V_{BUS}, 50 V/div.
CH2: V_{BPL}, 2 V/div.
CH3: V_{BPH}, 2 V/div.
CH4: V_{INL}, 1 V/div.
Time Scale: 1 ms/div.

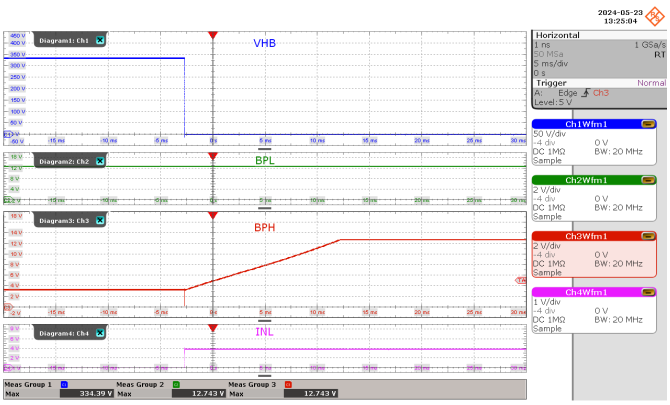

Figure 16 – BPL and BPH Signals at Start-up, INL HIGH.
CH1: V_{BUS}, 50 V/div.
CH2: V_{BPL}, 2 V/div.
CH3: V_{BPH}, 2 V/div.
CH4: V_{INL}, 1 V/div.
Time Scale: 5 ms/div.

7.1.2 Motor Start-Up Waveforms

The waveforms below demonstrate motor start-up at light load (100 mA) and full load (750 mA) conditions.

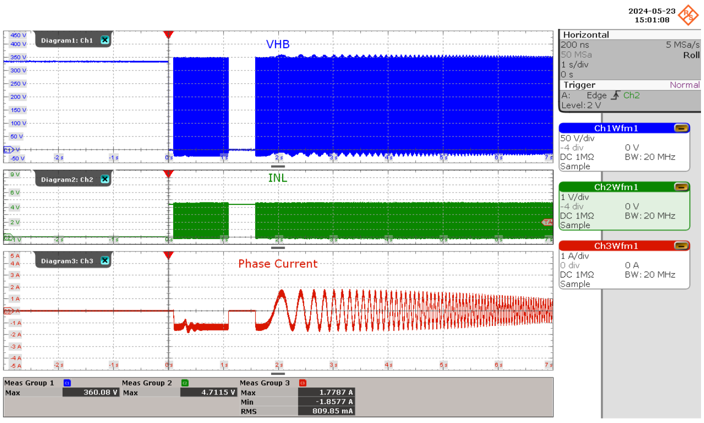

Figure 17 – Motor Start-up at 100 mA Load.
CH1: V_{HB}, 50 V/div.
CH2: V_{INL}, 1 V/div.
CH3: I_{PHASE}, 1 A/div.
Time Scale: 1 s/div.
Peak Phase Current = 1.86 A.

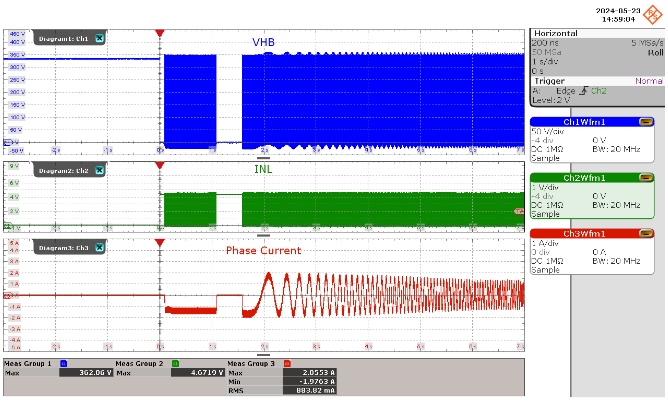

Figure 18 – Motor Start-up at 750 mA Load.
CH1: V_{HB}, 50 V/div.
CH2: V_{INL}, 1 V/div.
CH3: I_{PHASE}, 1 A/div.
Time Scale: 1 s/div.
Peak Phase Current = 2.06 A.

7.2 Steady-State Operation

7.2.1 Phase Voltages (Low-side V_{DS}) at Steady-State

The phase voltage (low-side V_{DS}) waveforms below were measured from light load to full load using a 10 kHz PWM signal, 340 V DC bus voltage, and at a motor speed of 3000 RPM.

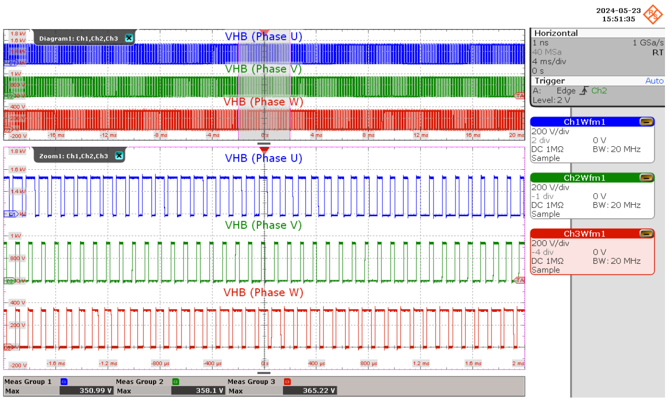

Figure 19 – Phase Voltages at 100 mA Load.
CH1: V_{HB_U}, 200 V/div.
CH2: V_{HB_V}, 200 V/div.
CH3: V_{HB_W}, 200 V/div.
Time Scale: 4 ms/div.
Peak Phase Voltage (U) = 351 V
Peak Phase Voltage (V) = 358 V
Peak Phase Voltage (W) = 365 V

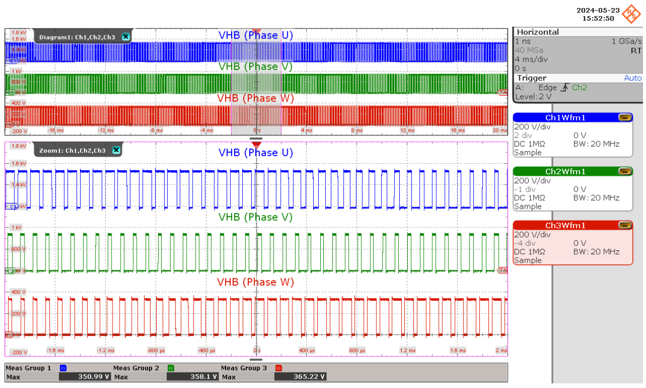

Figure 20 – Phase Voltages at 300 mA Load.
CH1: V_{HB_U}, 200 V/div.
CH2: V_{HB_V}, 200 V/div.
CH3: V_{HB_W}, 200 V/div.
Time Scale: 4 ms/div.
Peak Phase Voltage (U) = 351 V
Peak Phase Voltage (V = 358 V
Peak Phase Voltage (W) = 365 V

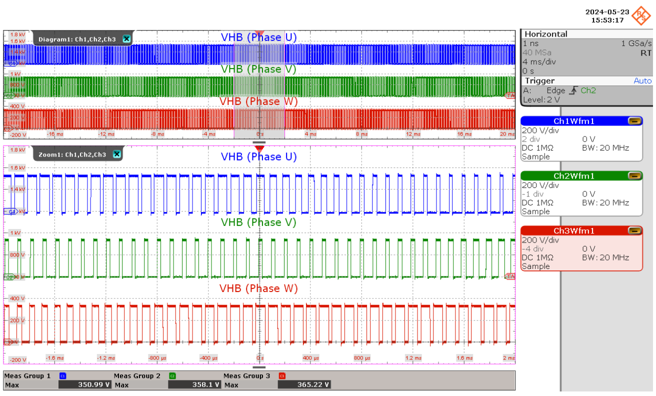

Figure 21 – Phase Voltages at 500 mA Load.
CH1: V_{HB_U}, 200 V/div.
CH2: V_{HB_V}, 200 V/div.
CH3: V_{HB_W}, 200 V/div.
Time Scale: 4 ms/div.
Peak Phase Voltage (U) = 351 V
Peak Phase Voltage (V) = 358 V
Peak Phase Voltage (W) = 365 V

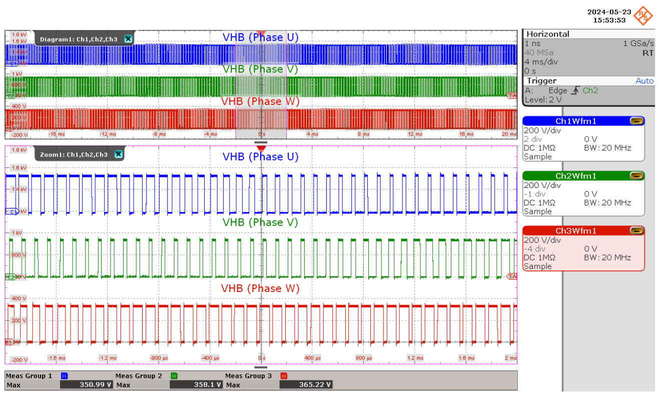

Figure 22 – Phase Voltages at 750 mA Load.
CH1: V_{HB_U}, 200 V/div.
CH2: V_{HB_V}, 200 V/div.
CH3: V_{HB_W}, 200 V/div.
Time Scale: 4 ms/div.
Peak Phase Voltage (U) = 351 V
Peak Phase Voltage (V) = 358 V
Peak Phase Voltage (W) = 365 V

7.2.2 Low-Side Drain-to-Source Voltage Slew Rate

The waveforms below show the voltage slew rate at the turn on and turn off transitions of the low-side FREDFET switching. These measurements were done at half load (375 mA) and full load (750 mA) operating conditions at the positive peak of the phase current.

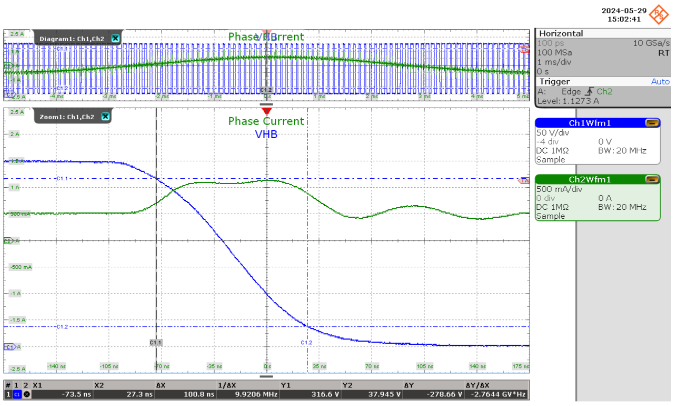

Figure 23 –Turn On Slew Rate, 375 mA Load.
CH1: V_{HB}, 50 V/div.
CH2: I_{PHASE}, 500 mA/div.
Time Scale: 1 ms/div.
Time Scale (Zoomed Area): 35 ns/div.
Measured Slew Rate = 2.76 V/ns.

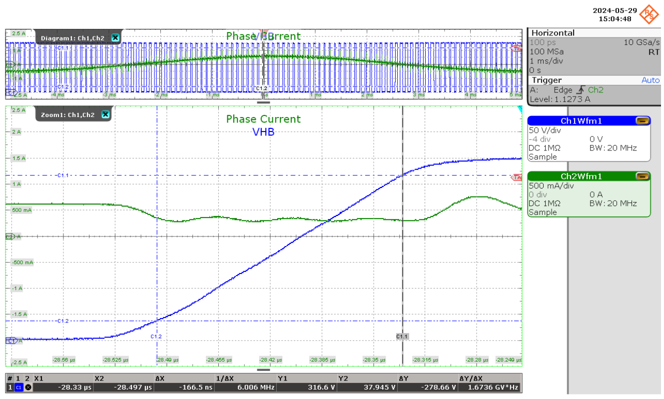

Figure 24 – Turn Off Slew Rate, 375 mA Load.
CH1: V_{HB}, 50 V/div.
CH2: I_{PHASE}, 500 mA/div.
Time Scale: 1 ms/div.
Time Scale (Zoomed Area): 35 ns/div.
Measured Slew Rate = 1.67 V/ns.

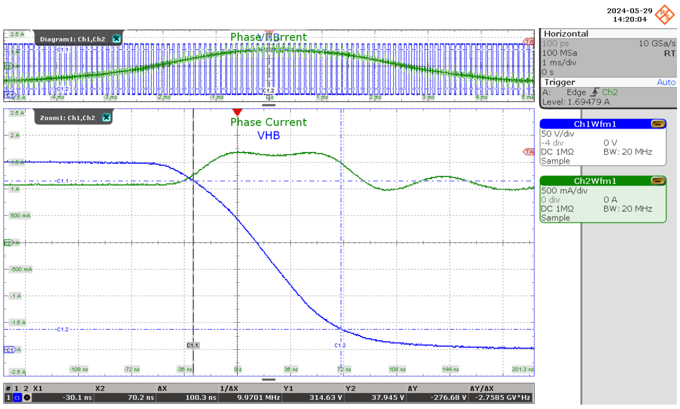

Figure 25 –Turn On Slew Rate, 750 mA Load.
CH1: V_{HB}, 50 V/div.
CH2: I_{PHASE}, 500 mA/div.
Time Scale: 1 ms/div.
Time Scale (Zoomed Area): 35 ns/div.
Measured Slew Rate = 2.76 V/ns.

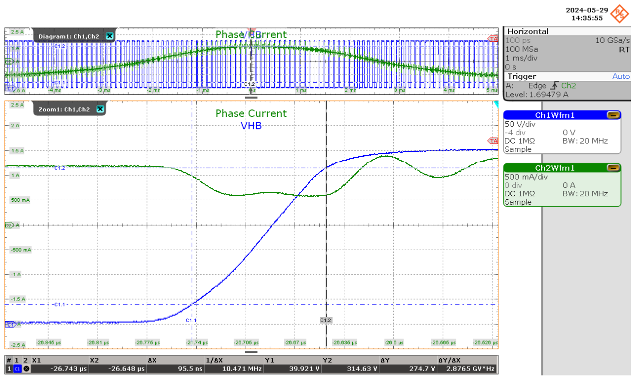

Figure 26 – Turn Off Slew Rate, 750 mA Load.
CH1: V_{HB}, 50 V/div.
CH2: I_{PHASE}, 500 mA/div.
Time Scale: 1 ms/div.
Time Scale (Zoomed Area): 35 ns/div.
Measured Slew Rate = 2.88 V/ns.

7.2.3 Phase Currents at Steady-State

The inverter phase currents using the three-phase modulation FOC algorithm are shown in the waveforms below. These were measured from light load to full load at steady-state operation.

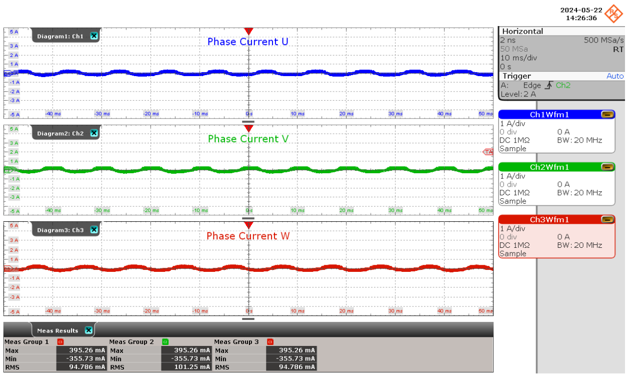

Figure 27 – Phase Current at 100 mA Load.
CH1: IPHASEU, 1 A/div.
CH2: IPHASEV, 1 A/div.
CH3: IPHASEW, 1 A/div.
Time Scale: 10 ms/div.
RMS Current (U) = 95 mARMS.
RMS Current (V) = 101 mARMS.
RMS Current (W) = 95 mARMS.

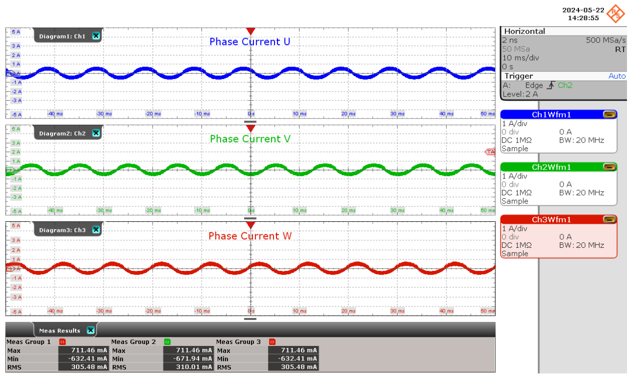

Figure 28 – Phase Current at 300 mA Load.
CH1: IPHASEU, 1 A/div.
CH2: IPHASEV, 1 A/div.
CH3: IPHASEW, 1 A/div.
Time Scale: 10 ms/div.
RMS Current (U) = 305 mARMS.
RMS Current (V) = 310 mARMS.
RMS Current (W) = 305 mARMS.

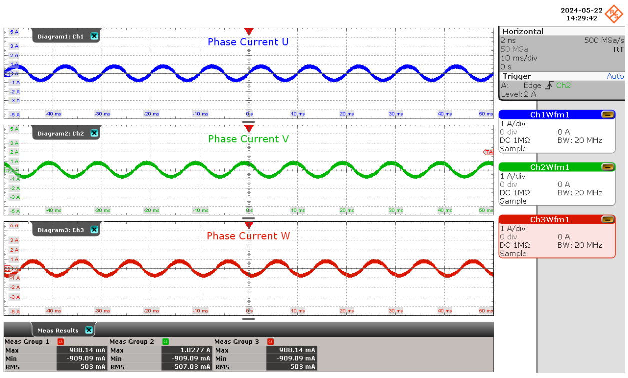

Figure 29 – Phase Current at 500 mA Load.
CH1: IPHASEU, 1 A/div.
CH2: IPHASEV, 1 A/div.
CH3: IPHASEW, 1 A/div.
Time Scale: 10 ms/div.
RMS Current (U) = 503 mARMS.
RMS Current (V) = 507 mARMS.
RMS Current (W) = 503 mARMS.

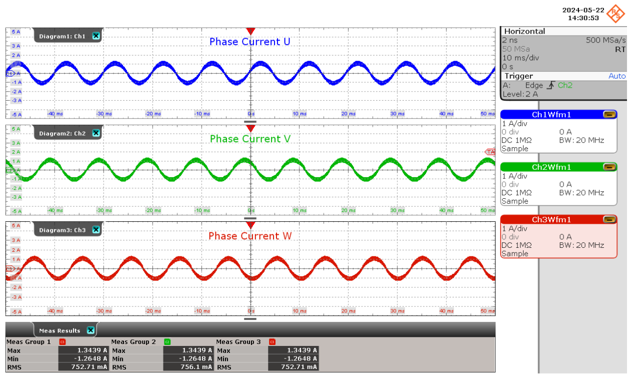

Figure 30 – Phase Current at 750 mA Load.
CH1: IPHASEU, 1 A/div.
CH2: IPHASEV, 1 A/div.
CH3: IPHASEW, 1 A/div.
Time Scale: 10 ms/div.
RMS Current (U) = 753 mARMS.
RMS Current (V) = 756 mARMS.
RMS Current (W) = 753 mARMS.

7.2.4 PWM Input Signals at Steady-State

The waveforms below show the low-side (INL) and high-side (/INH) PWM signals from light load to full load conditions at steady-state operation. The PWM frequency is set at 10 kHz with a constant motor speed of 3000 RPM.

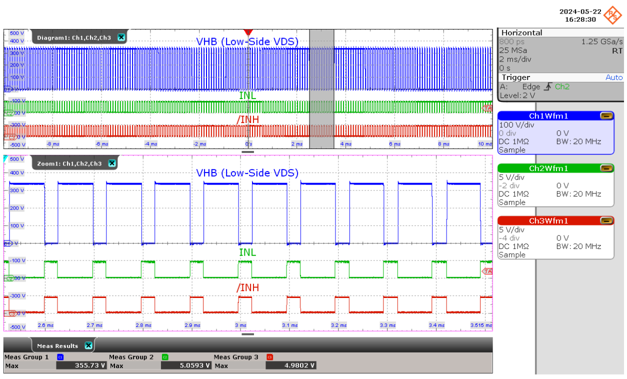

Figure 31 – INL and /INH Signals at 100 mA Load.
CH1: V_{HB}, 100 V/div.
CH2: V_{INL}, 5 V/div.
CH3: V_{INH}, 5 V/div.
Time Scale: 2 ms/div.
Time Scale (Zoomed Area): 100 µs/div.

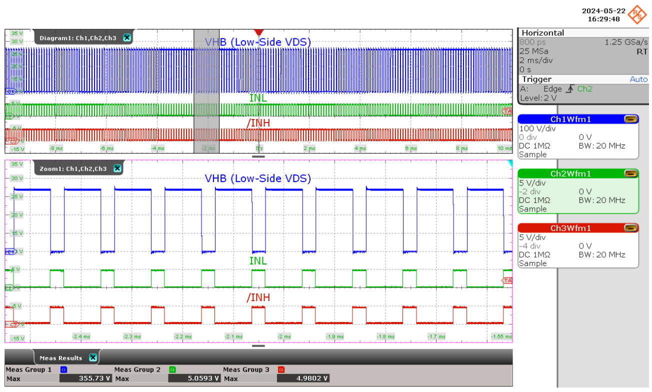

Figure 32 – INL and /INH Signals at 300 mA Load.
CH1: V_{HB}, 100 V/div.
CH2: V_{INL}, 5 V/div.
CH3: V_{INH}, 5 V/div.
Time Scale: 2 ms/div.
Time Scale (Zoomed Area): 100 µs/div.

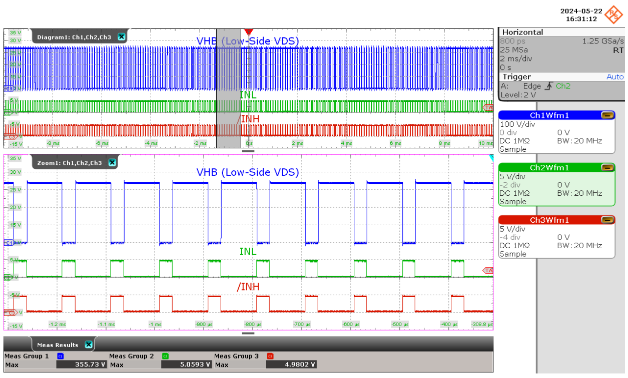

Figure 33 – INL and /INH Signals at 500 mA Load.
CH1: V_{HB}, 100 V/div.
CH2: V_{INL}, 5 V/div.
CH3: V_{INH}, 5 V/div.
Time Scale: 2 ms/div.
Time Scale (Zoomed Area): 100 µs/div.

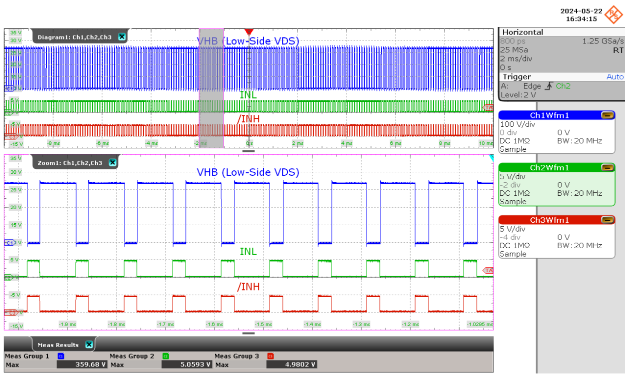

Figure 34 – INL and /INH Signals at 750 mA Load.
CH1: V_{HB}, 100 V/div.
CH2: V_{INL}, 5 V/div.
CH3: V_{INH}, 5 V/div.
Time Scale: 2 ms/div.
Time Scale (Zoomed Area): 100 µs/div.

7.2.5 BPL and BPH at Steady-State

The waveforms below show the bypass supply voltage DC levels from light load to full load condition using self-supply mode in steady-state operation.

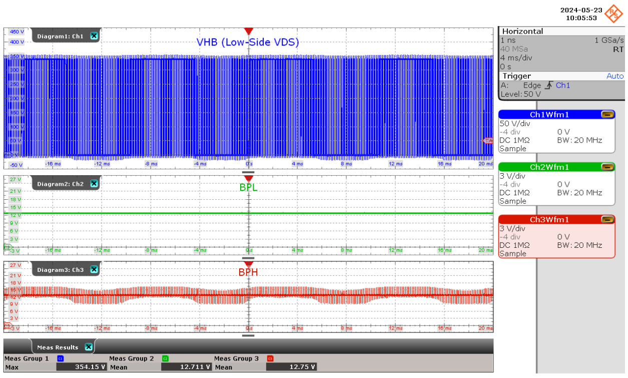

Figure 35 – BPL and BPH Signals at 100 mA Load.
CH1: V_{HB}, 50 V/div.
CH2: V_{BPL}, 3 V/div.
CH3: V_{BPH}, 3 V/div.
Time Scale: 4 ms/div.
BPL Average Voltage = 12.7 V.
BPH Average Voltage = 12.8 V.

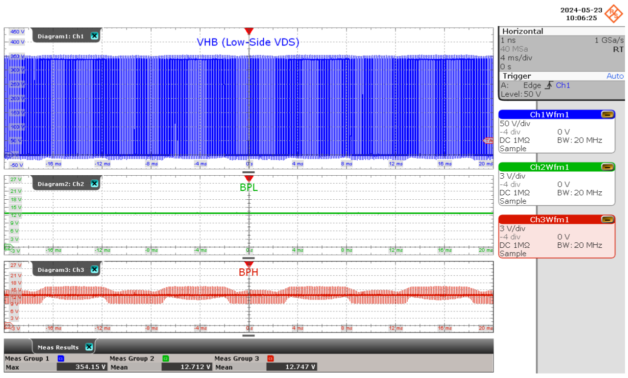

Figure 36 – BPL and BPH Signals at 300 mA Load.
CH1: V_{HB}, 50 V/div.
CH2: V_{BPL}, 3 V/div.
CH3: V_{BPH}, 3 V/div.
Time Scale: 4 ms/div.
BPL Average Voltage = 12.7 V.
BPH Average Voltage = 12.8 V.

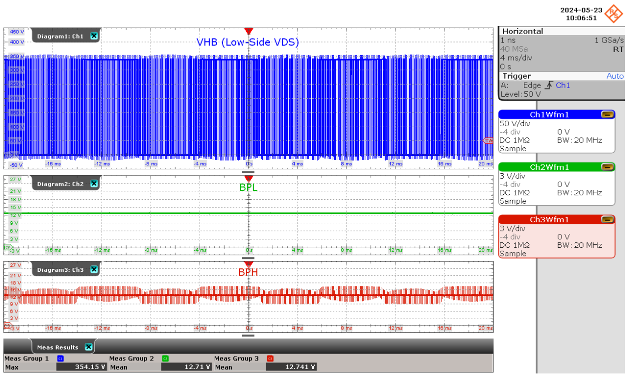

Figure 37 – BPL and BPH Signals at 500 mA Load.
CH1: V_{HB}, 50 V/div.
CH2: V_{BPL}, 3 V/div.
CH3: V_{BPH}, 3 V/div.
Time Scale: 4 ms/div.
BPL Average Voltage = 12.7 V.
BPH Average Voltage = 12.7 V.

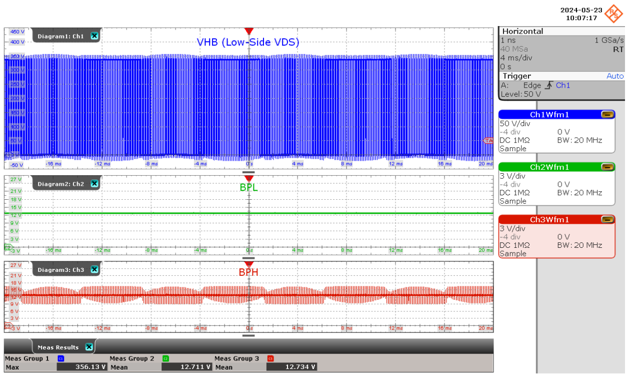

Figure 38 – BPL and BPH Signals at 750 mA Load.
CH1: V_{HB}, 50 V/div.
CH2: V_{BPL}, 3 V/div.
CH3: V_{BPH}, 3 V/div.
Time Scale: 4 ms/div.
BPL Average Voltage = 12.7 V.
BPH Average Voltage = 12.7 V.

7.3 Thermal Performance

Provided are thermal scans showing the BridgeSwitch-2 device case temperatures at 100 mA, 385 mA, and 750 mA loading conditions in self and external supply modes of operation. These measurements were recorded at 340 VDC with the inverter being driven by a 10 kHz PWM signal implementing the three-phase modulation FOC algorithm at a constant motor speed of 3000 RPM. Case temperatures were recorded after a thirty-minute soak time to ensure steady-state conditions were reached. Throughout these tests, an average ambient of 29 ºC was observed with the board under test enclosed in an acrylic case to minimize the effects of air flow.

To solely reflect the inverter temperature, the input diode, shunt resistors, 15 V auxiliary supply, and 5 V linear regulator were disabled by shorting input diode D6 and shunt resistors R29, R35, and R42, and depopulating auxiliary supply devices U4 and U5. The microcontroller VDD supply (5 V) was used to pull up the EF pin, while an external low-voltage DC supply provides 15 V during external supply mode. Section 8.5 of the Appendix explains the IPH reconstruction by the MotorXpert Suite in detail allowing the IPH signal to be used as current feedback for this application.

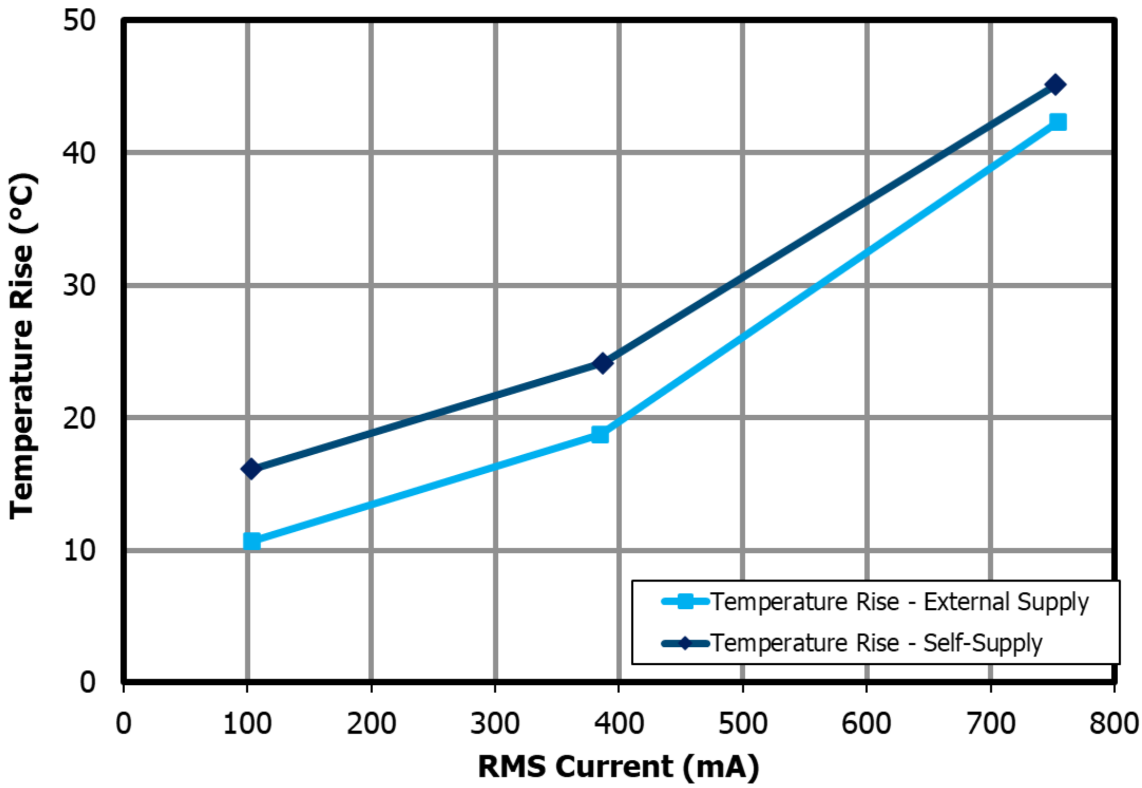

Figure 39 – Temperature Rise using Self and External Supply Mode.

7.3.1 100 mA Average Motor Phase Current

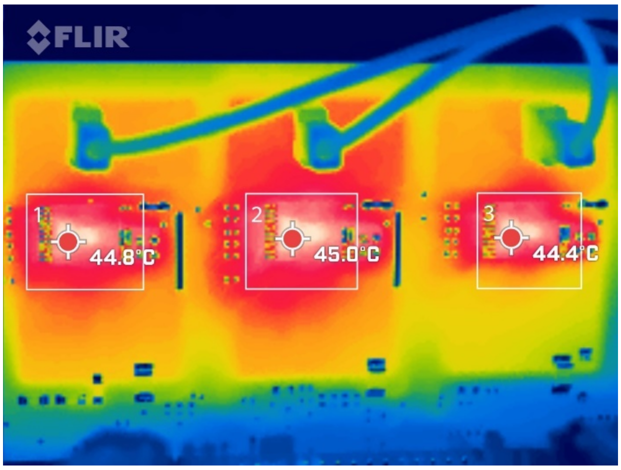

Figure 40 – BridgeSwitch-2 Case Temperature at 100 mA Phase Current (Self-Supply Mode).

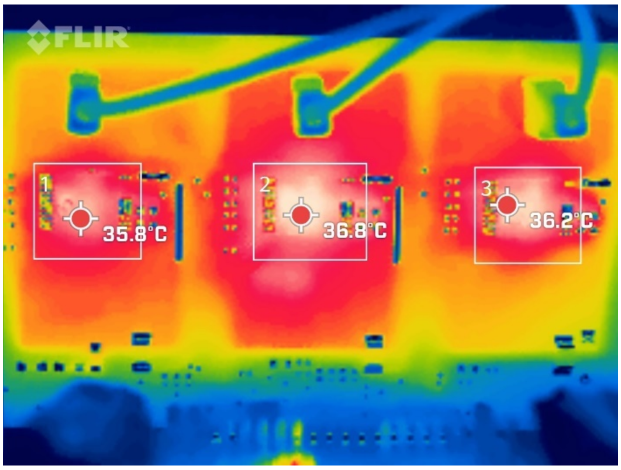

Figure 41 – BridgeSwitch-2 Case Temperature at 100 mA Phase Current (External Supply Mode).

7.3.2 385 mA Average Motor Phase Current

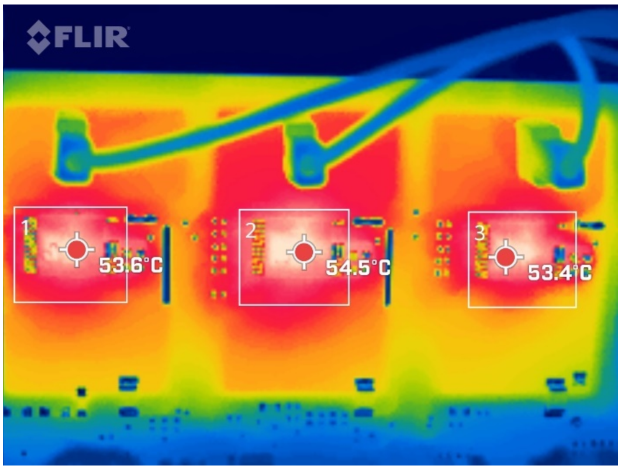

Figure 42 – BridgeSwitch-2 Case Temperature at 385 mA Phase Current (Self-Supply Mode).

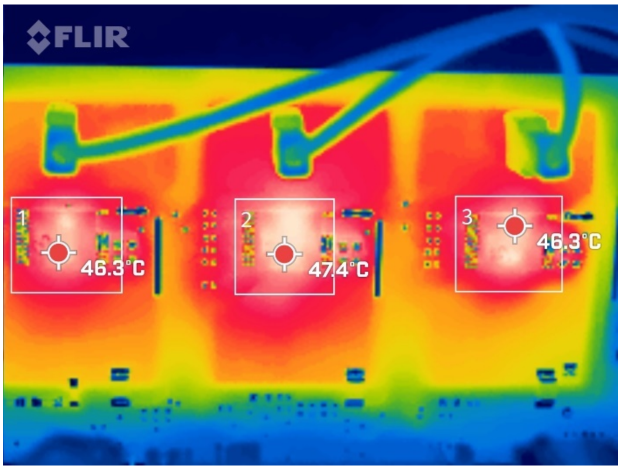

Figure 43 – BridgeSwitch-2 Case Temperature at 385 mA Phase Current (External Supply Mode).

7.3.3 750 mA Average Motor Phase Current

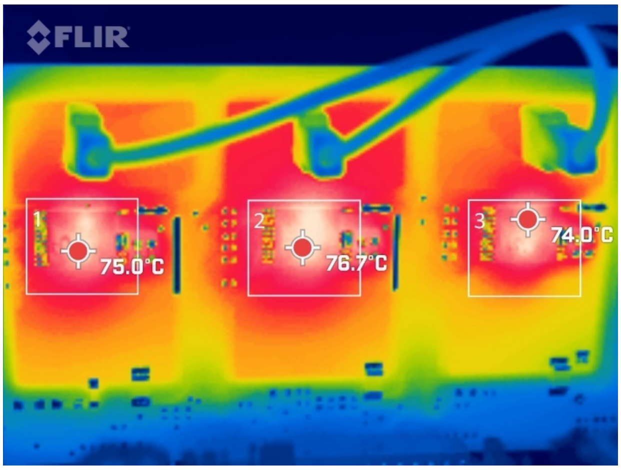

Figure 44 – BridgeSwitch-2 Case Temperature at 750 mA Phase Current (Self-Supply Mode).

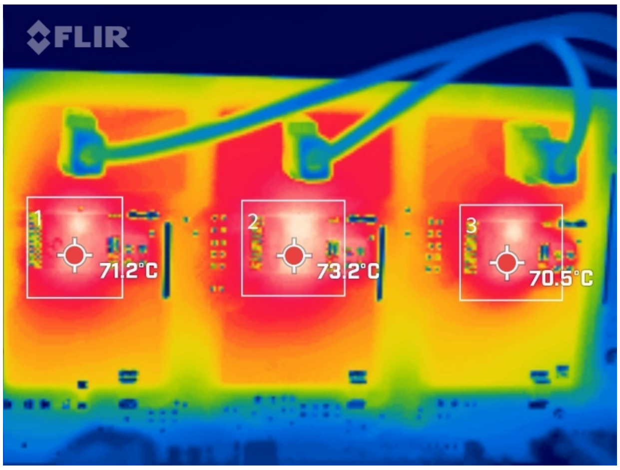

Figure 45 – BridgeSwitch-2 Case Temperature at 750 mA Phase Current (External Supply Mode).

7.3.4 Thermal Scan Summary Tables

7.3.4.1 Self-Supply Mode

Phase	Device	Phase Current		
		100 mA	**385 mA**	**750 mA**
U	U1	44.8 °C	53.6 °C	75.0 °C
V	U2	45.0 °C	54.5 °C	76.7 °C
W	U3	44.4 °C	53.4 °C	74.0 °C
Average Temperature		**44.7 °C**	**53.8 °C**	**75.2 °C**
Ambient Temperature		28.6 °C	29.7 °C	30.1 °C
Temperature Rise		**16.1 °C**	**24.1 °C**	**45.1 °C**

Table 3 – Thermal Scan Summary Table (Self-Supply Mode).

7.3.4.2 External Supply Mode

Phase	Device	Phase Current		
		100 mA	**385 mA**	**750 mA**
U	U1	35.8 °C	46.3 °C	71.2 °C
V	U2	36.8 °C	47.4 °C	73.2 °C
W	U3	36.2 °C	46.3 °C	70.5 °C
Average Temperature		**36.3 °C**	**46.7 °C**	**71.6 °C**
Ambient Temperature		25.6 °C	27.9 °C	29.3 °C
Temperature Rise		**10.7 °C**	**18.8 °C**	**42.3 °C**

Table 4 – Thermal Scan Summary Table (External Supply Mode).

7.4 No-Load Input Power Consumption

7.4.1 Self-Supply (Sleep Mode OFF)

Shown below is the inverter no-load input power measured across the operating DC bus range during self-supply mode and with sleep mode disabled. This test uses the setup shown in Figure 68 of the Appendix. To solely reflect the inverter standby power consumption, the input diode, DC bus monitoring resistors, 15 V auxiliary circuit, and 5 V linear regulator were disabled by shorting input diode D6, and depopulating bus sensing resistors R21, R22, R23, and auxiliary supply devices U4 and U5.

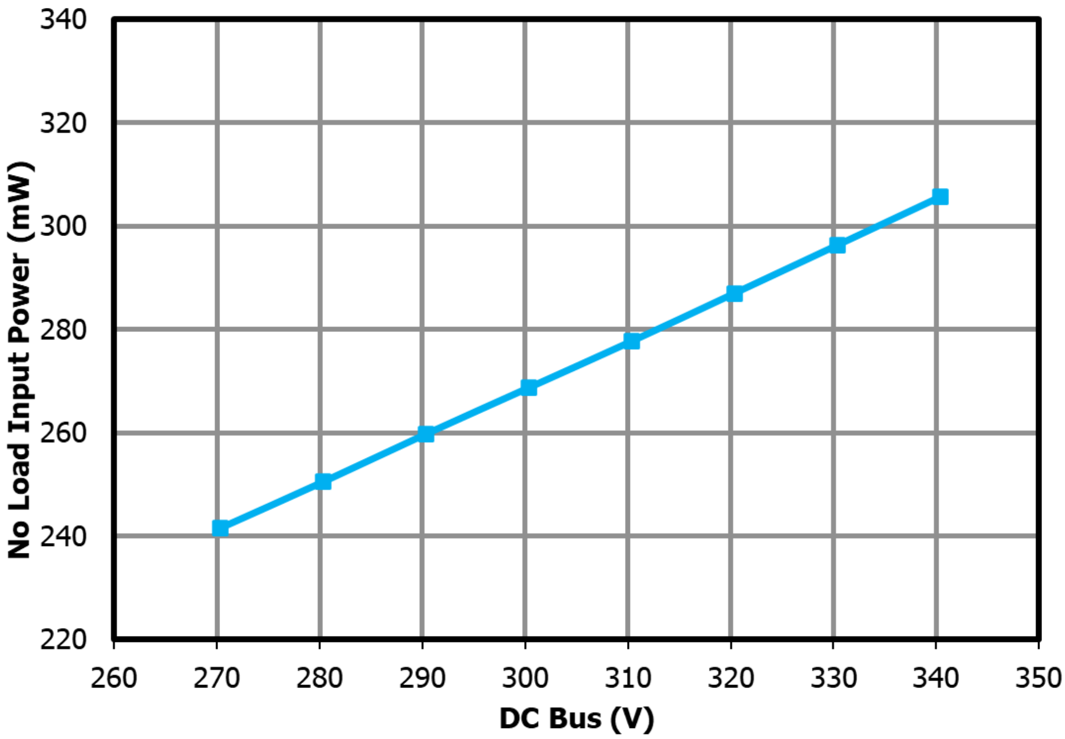

Figure 46 – No-Load Input Power (Sleep OFF).

7.4.2 Self-Supply (Sleep Mode ON)

BridgeSwitch-2 features sleep mode designed to greatly reduce the standby input power consumption by disabling the low-side driver functionality during non-operation. This is enabled by setting the SLP pin voltage HIGH (min. 2.5 V).

Like the previous graph, these measurements use the no-load input power measurement setup in Figure 68 of the Appendix. To solely reflect the inverter standby power consumption, the input diode, DC bus sensing circuit, 15 V auxiliary circuit, and 5 V linear regulator were disabled by shorting input diode D6, and depopulating bus sensing resistors R21, R22, R23, and auxiliary supply devices U4 and U5.

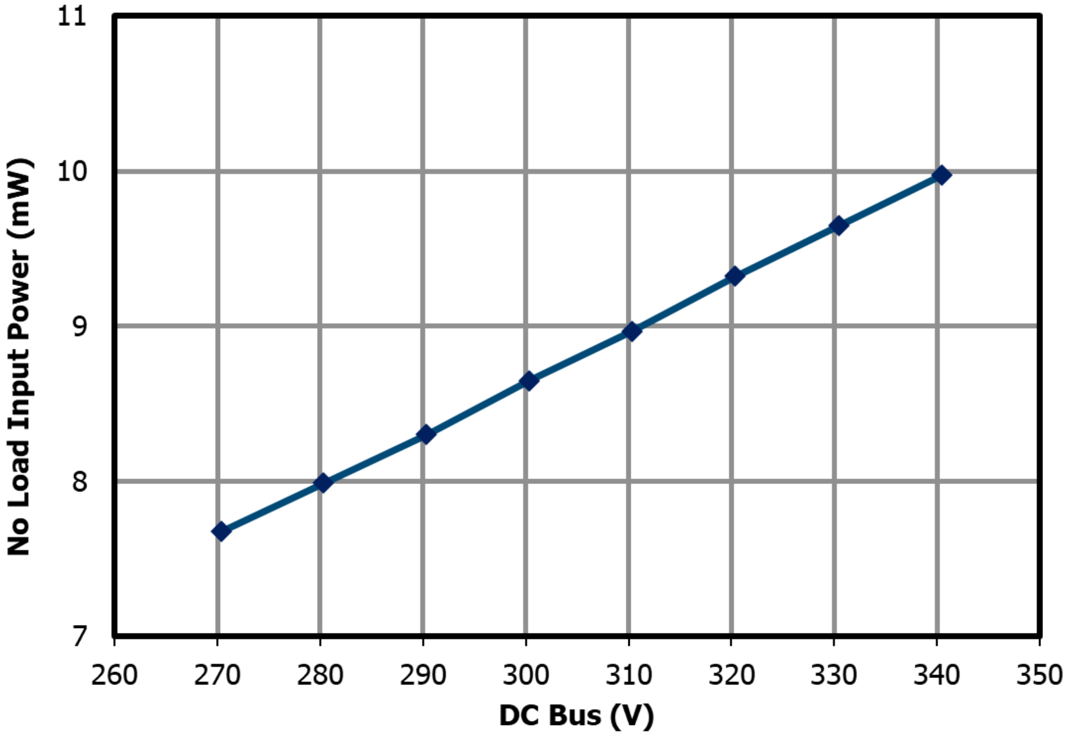

Figure 47 – No-Load Input Power (Sleep ON).

The standby power consumption difference after enabling sleep mode is shown below:

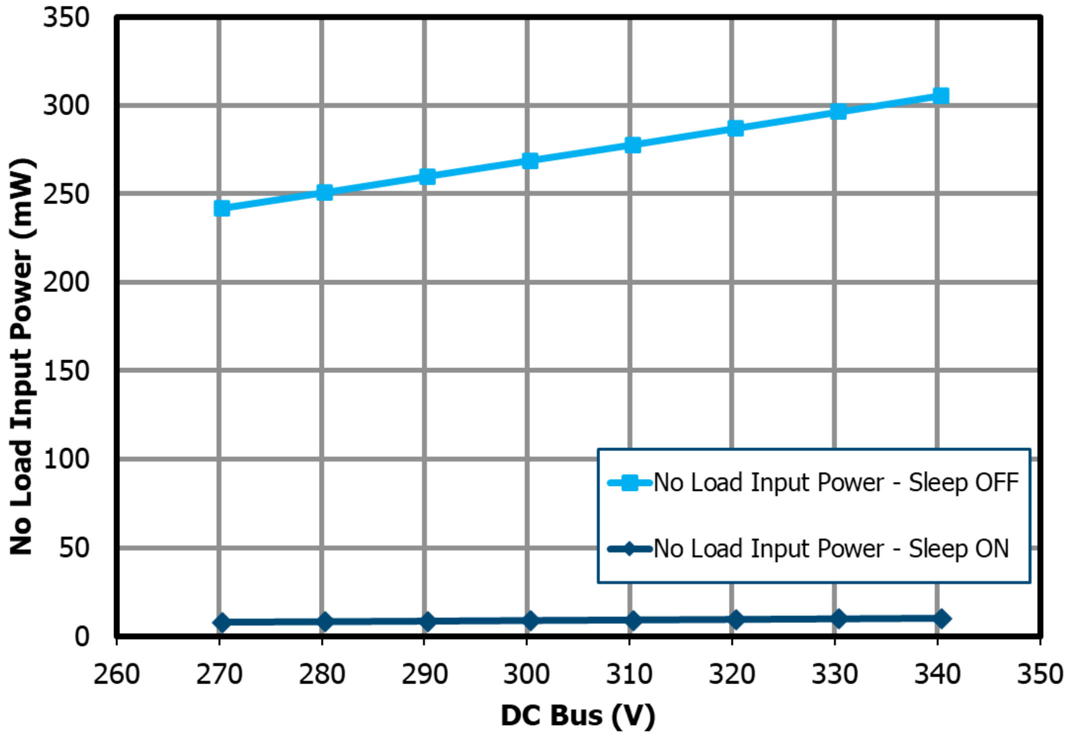

Figure 48 – No-Load Input Power Comparison (Sleep Mode ON vs. OFF)

7.5 Efficiency

Shown below is the BridgeSwitch-2 inverter efficiency data from light load to full load at both self and external supply modes of operation. A soak time of fifteen minutes per loading condition was maintained to ensure steady-state conditions were achieved. These measurements were made at 340 VDC with the inverter driven by a 10 kHz PWM signal implementing the three-phase FOC modulation algorithm at a constant motor speed of 3000 RPM.

To solely reflect the inverter efficiency, the input diode, shunt resistors, 15 V auxiliary supply, and 5 V linear regulator were disabled by shorting input diode D6 and shunt resistors R29, R35, and R42, and depopulating auxiliary supply devices U4 and U5. The microcontroller VDD supply (5 V) was used to pull up the EF pin, while an external low-voltage DC supply provides 15 V during external supply mode. Section 8.5 of the Appendix explains the IPH reconstruction by the MotorXpert Suite in detail allowing the IPH signal to be used as current feedback for this application.

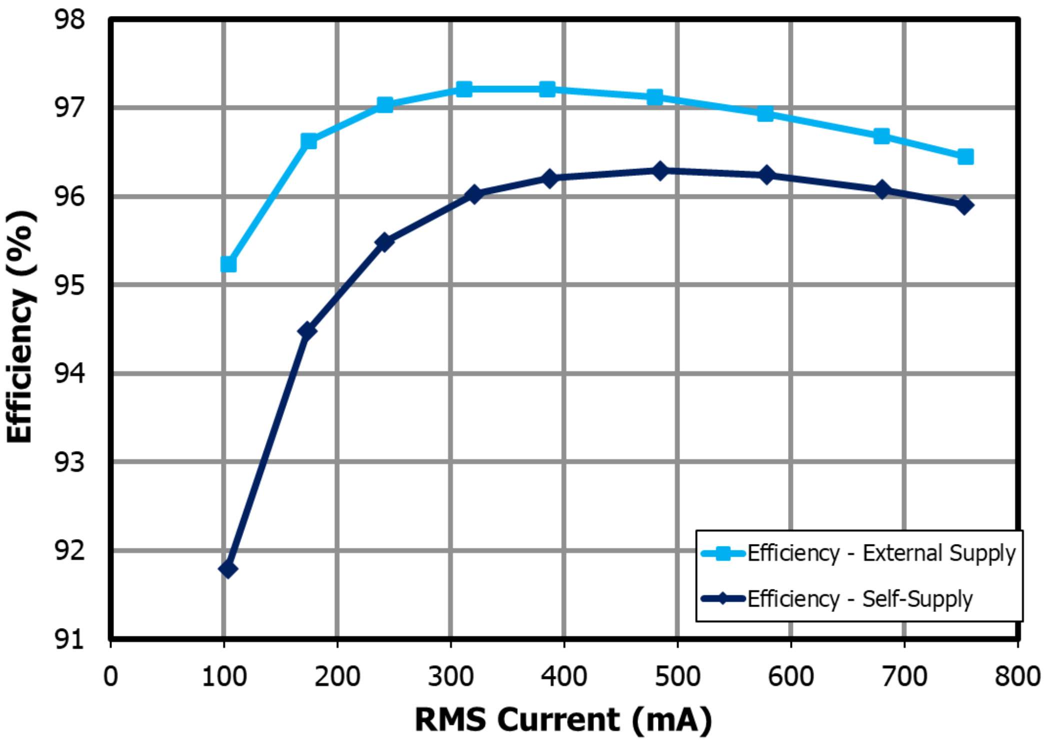

Figure 49 – Inverter Efficiency Graph.

7.5.1 Efficiency Table at Self Supply Mode

DC Input Voltage (V_{IN})	Input DC Current (mA)	Input Power (W)	I_{RMS}U (mA)	I_{RMS}V (mA)	I_{RMS}W (mA)	Inverter Output Power (W)	Inverter Efficiency (%)
340	171	22	100	106	103	20	91.8
340	192	36	170	179	172	34	94.5
340	217	49	240	248	239	47	95.5
340	252	65	321	324	318	63	96.0
340	283	78	388	388	385	75	96.2
340	333	98	487	485	482	95	96.3
340	385	118	581	580	576	113	96.2
340	442	139	682	682	678	133	96.1
340	483	153	754	754	750	147	95.9

Table 5 – Efficiency Table (Self-Supply Mode).

7.5.2 Efficiency Table at External Supply Mode

DC Input Voltage (V_{IN})	Input DC Current (mA)	Input Power (W)	I_{RMS}U (mA)	I_{RMS}V (mA)	I_{RMS}W (mA)	Inverter Output Power (W)	Inverter Efficiency (%)
340	112	21	101	107	104	20	95.2
340	140	35	171	180	173	34	96.6
340	172	49	240	247	239	47	97.0
340	207	62	311	315	309	61	97.2
340	247	77	386	387	383	75	97.2
340	300	96	481	480	478	94	97.1
340	357	116	580	578	575	113	96.9
340	418	138	681	682	678	133	96.7
340	461	153	755	756	752	147	96.4

Table 6 – Efficiency Table (External Supply Mode).

7.6 Device and System Level Protection

BridgeSwitch-2 features a new Error Flag (EF) which offers simplified fault handling. It is set to HIGH during normal operation and is automatically pulled LOW by destructive faults such as over-temperature, overvoltage, and sustained overcurrent faults. This inhibits switching for all devices until either an EF latch reset signal or upon reaching the hysteresis level. A full motor start-up sequence is required to resume normal operation afterwards.

7.6.1 Cycle-by-Cycle Overcurrent Protection (OCP)

The current limiting function of the BridgeSwitch-2 device is demonstrated below by increasing the open-loop duty cycle during the start-up phase. For the first set of waveforms, the default current limit of 2.5 A_{PK} was maintained. Minor clipping of the phase current can be observed on Figure 50 as the phase current slightly exceeds the current limit. With the current limit decreased to 60% of its default value (1.7 A_{PK}), the clipping becomes more apparent as seen on Figure 51.

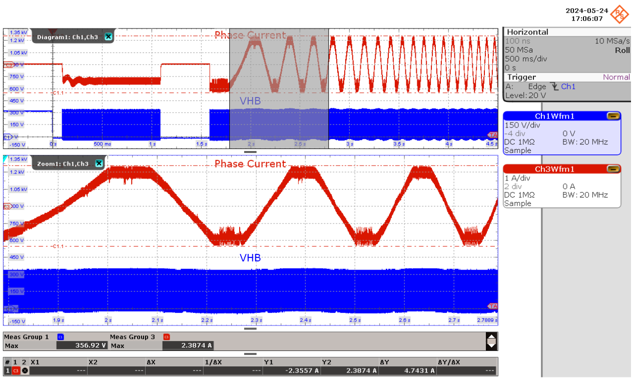

Figure 50 – Overcurrent Operation, I_{LIM} = 2.50 A.
CH3: I_{PHASE}, 1 A/div.
CH1: V_{HB}, 150 V/div.
Time Scale: 500 ms/div.
Peak Phase Current = 2.39 A

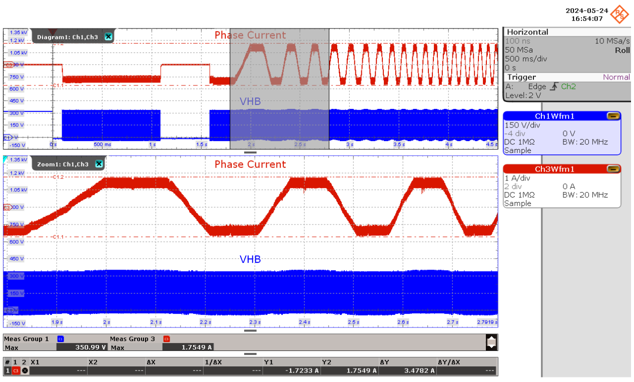

Figure 51 – Overcurrent Operation, I_{LIM} = 1.70 A.
CH3: I_{PHASE}, 1 A/div.
CH1: V_{HB}, 150 V/div.
Time Scale: 500 ms/div.
Peak Phase Current = 1.75 A

7.6.2 Over-temperature Protection

The waveform below depicts the low-side FREDFET over-temperature shutdown. An external heat source was applied to a single BridgeSwitch-2 device increasing the case temperature to the thermal shutdown threshold (150 °C).

7.6.2.1 Hysteretic Thermal Shutdown

The default SLP resistor (9.53 kΩ) sets the thermal shutdown response to hysteretic. This allows the inverter to restart switching once the device temperature drops below the hysteresis level. The EF bus inhibits switching for all devices when pulled LOW, and automatically goes HIGH once the device temperature is within the safe operating range.

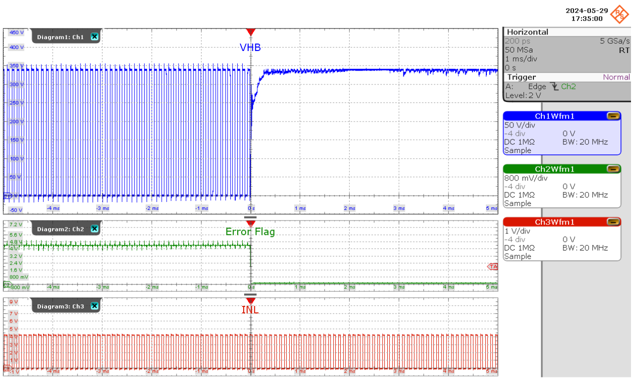

Figure 52 – Hysteretic Thermal Shutdown.
CH1: V_{HB}, 50 V/div.
CH2: V_{EF}, 800 mV/div.
CH3: V_{INL}, 1 V/div.
Time Scale: 1 ms/div.

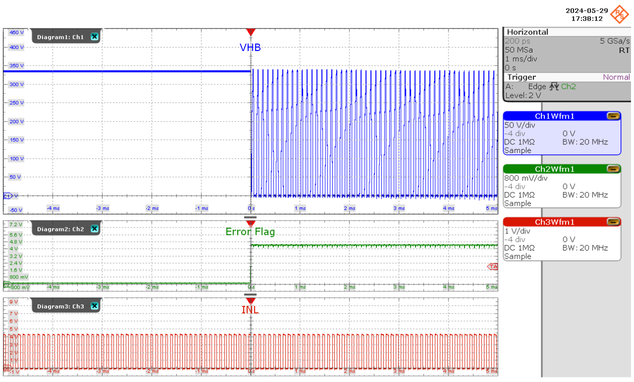

Figure 53 – Hysteretic Thermal Shutdown Reset.
CH1: V_{HB}, 50 V/div.
CH2: V_{EF}, 800 mV/div.
CH3: V_{INL}, 1 V/div.
Time Scale: 1 ms/div.

7.6.2.2 Latching Thermal Shutdown

Depopulating the SLP programming resistor (≥1 MΩ) or replacing it with a 133 kΩ resistor sets the thermal shutdown response to latching. Shown below is the latching thermal shutdown response followed by an EF reset signal. For this configuration, switching is inhibited for all devices connected to the EF bus until either an EF reset signal is received, or a power recycle is performed.

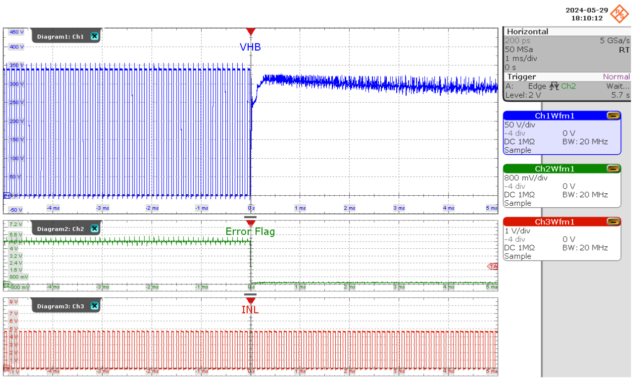

Figure 54 – Latching Thermal Shutdown.
CH1: V_{HB}, 50 V/div.
CH2: V_{EF}, 800 mV/div.
CH3: V_{INL}, 1 V/div.
Time Scale: 1 ms/div.

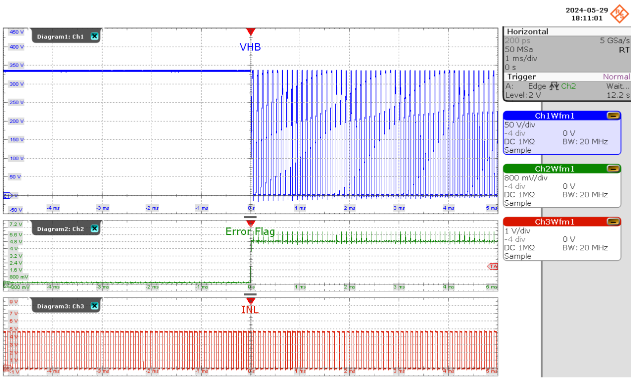

Figure 55 – Latching Thermal Shutdown Reset (EF Reset Signal).
CH1: V_{HB}, 50 V/div.
CH2: V_{EF}, 800 mV/div.
CH3: V_{INL}, 1 V/div.
Time Scale: 1 ms/div.

7.6.3 Overvoltage Protection (OVP)

The waveforms below depict the bus voltage monitoring feature with the overvoltage threshold set to 362 VDC through the total resistance value of components R21, R22, and R23 (6 MΩ). Device switching is inhibited when the EF pin voltage is pulled down after exceeding the overvoltage threshold. Switching resumes once the bus voltage level drops below the overvoltage hysteresis level, automatically pulling the EF voltage HIGH.

Due to the common EF connection between the BridgeSwitch-2 devices, all device switching is inhibited ensuring reliable protection against destructive faults. A full start-up cycle is required to resume normal operation afterwards.

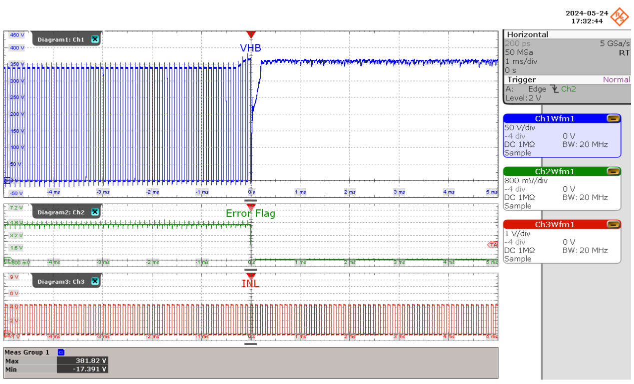

Figure 56 – OVP, 340 V to 362 V.
CH1: V_{HB}, 50 V/div.
CH2: V_{EF}, 800 mV/div.
CH3: V_{INL}, 1 V/div.
Time Scale: 1 ms/div.
Measured OVP Level = 362 V.

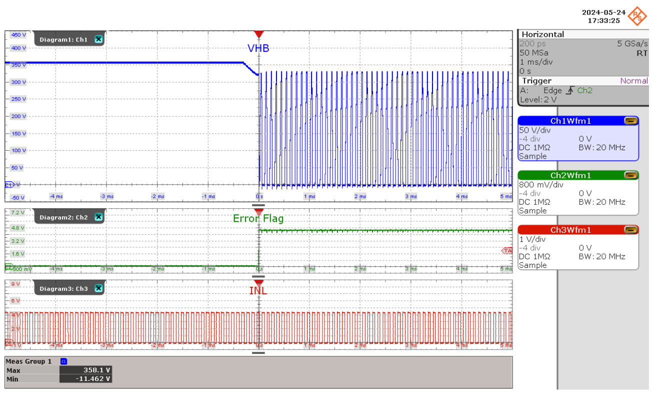

Figure 57 – OVP Clear, 362 V to 333 V.
CH1: V_{HB}, 50 V/div.
CH2: V_{EF}, 800 mV/div.
CH3: V_{INL}, 1 V/div.
Time Scale: 1 ms/div.
Measured OVP Hysteresis Level = 333 V.

7.7 Abnormal Motor Operation Test

This section presents the abnormal operation test results for appliances with motors as described in IEC 60335-1 (Safety of household and similar electrical appliances). It includes the following tests:

- Operation under stalled motor conditions
- Operation with one motor winding disconnected
- Running overload test

The test results demonstrate the integrated protection features of the BridgeSwitch-2 under these abnormal conditions.

7.7.1 Operation under Stalled Motor Conditions

For this test, the inverter was set to initially run at 340 VDC, with a phase current of 375 mA and 750 mA, and a motor speed of 3000 RPM. After steady-state conditions are achieved, the load was increased drastically to simulate sudden braking of the motor. Once the motor stalls, the overcurrent protection of the BridgeSwitch-2 device engages, and no damage is observed on both the inverter board and the motor. The resulting waveforms are shown below:

Stalled Condition at 375 mA Load

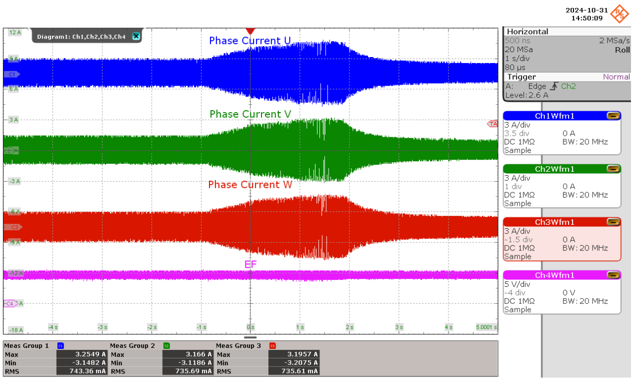

Figure 58 – Stalled Motor Condition, 375 mA Load.
CH1: $I_{PHASE(U)}$, 3 A/div.
CH2: $I_{PHASE(V)}$, 3 A/div.
CH3: $I_{PHASE(W)}$, 3 A/div.
CH4: V_{EF}, 5 V/div.
Time Scale: 1 s/div.

Stalled Condition at 750 mA Load

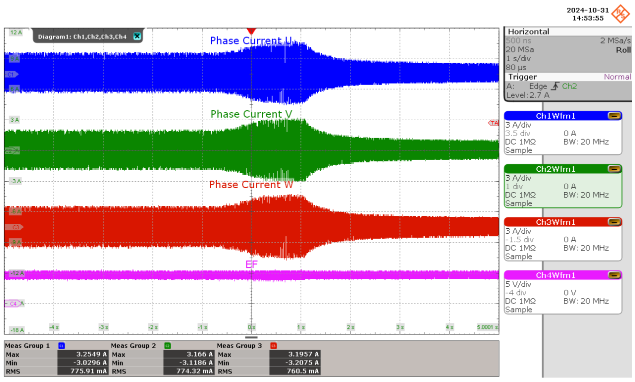

Figure 59 – Stalled Motor Condition, 750 mA Load.
CH1: $I_{PHASE(U)}$, 3 A/div.
CH2: $I_{PHASE(V)}$, 3 A/div.
CH3: $I_{PHASE(W)}$, 3 A/div.
CH4: V_{EF}, 5 V/div.
Time Scale: 1 s/div.

7.7.2 Operation with One Motor Winding Disconnected

For this test, the inverter was set to initially run at 340 VDC, with a phase current of 375 mA and 750 mA, and a motor speed of 3000 RPM. After steady-state conditions are achieved, one motor winding is disconnected through a switch.

At half load (375 mA), motor operation continues with increased phase current levels on the remaining motor phases. Reconnecting the motor winding reverts the operating conditions back to its initial state.

At full load (750 mA), the overcurrent protection is triggered after disconnecting one phase causing the motor to stall. The full start-up sequence is required after reconnection to run the motor normally. No damage was incurred by both the BridgeSwitch-2 inverter board and motor during and after this test.

Phase U Disconnected at Half Load

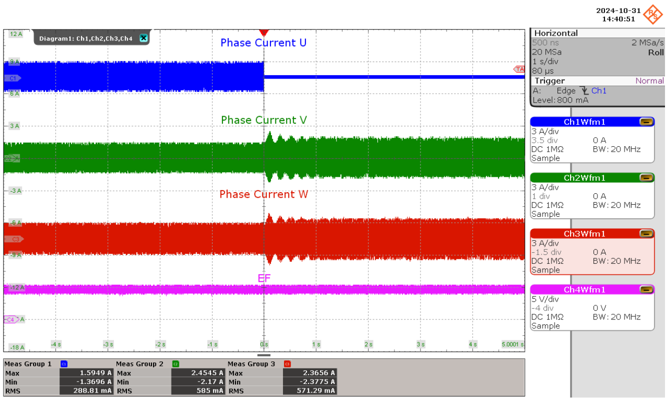

Figure 60 – Motor Winding Disconnection, Half Load.
CH1: $I_{PHASE(U)}$, 3 A/div.
CH2: $I_{PHASE(V)}$, 3 A/div.
CH3: $I_{PHASE(W)}$, 3 A/div.
CH4: V_{EF}, 5 V/div.
Time Scale: 1 s/div.

Phase U Reconnected at Half Load

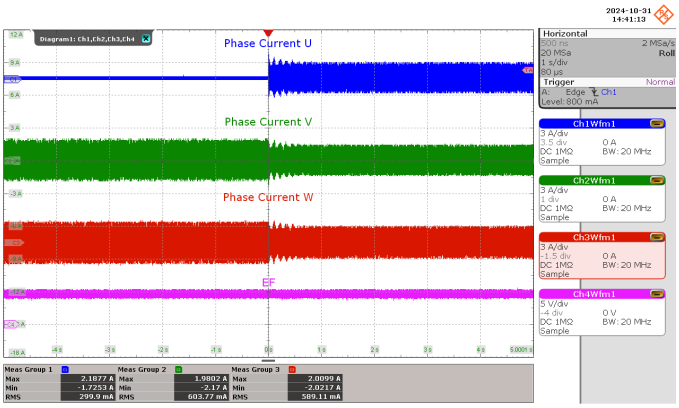

Figure 61 – Motor Winding Reconnection, Half Load.
CH1: $I_{PHASE(U)}$, 3 A/div.
CH2: $I_{PHASE(V)}$, 3 A/div.
CH3: $I_{PHASE(W)}$, 3 A/div.
CH4: V_{EF}, 5 V/div.
Time Scale: 1 s/div.

Phase U Disconnected at Full Load

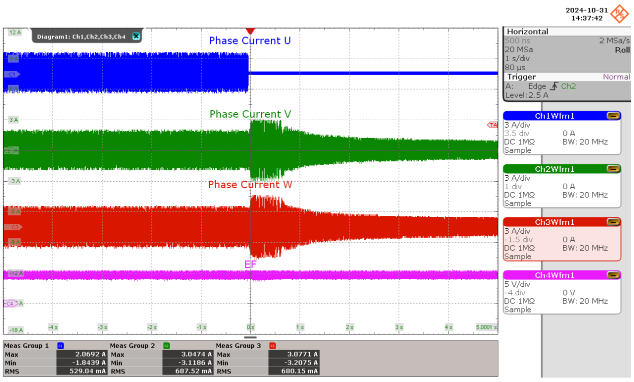

Figure 62 – Motor Winding Disconnection, Full Load.

CH1: $I_{PHASE(U)}$, 3 A/div.
CH2: $I_{PHASE(V)}$, 3 A/div.
CH3: $I_{PHASE(W)}$, 3 A/div.
CH4: V_{EF}, 5 V/div.
Time Scale: 1 s/div.

Note: At full load, the motor stalls after one motor winding is disconnected and maintains its stalled condition after the motor winding is reconnected.

7.7.3 Running Overload Test

The running overload test is performed by gradually increasing the current through the motor windings until the motor stalls. For this test, the increase is done in ten percent increments and steady-state conditions are achieved each time. This is repeated until the motor stops spinning.

Figure 63 displays the motor phase currents at the overloaded conditions until the motor stalls. No damage is incurred by both the BridgeSwitch-2 inverter board and motor during and after this test.

Running Overload Test > 1.5 A_{rms}

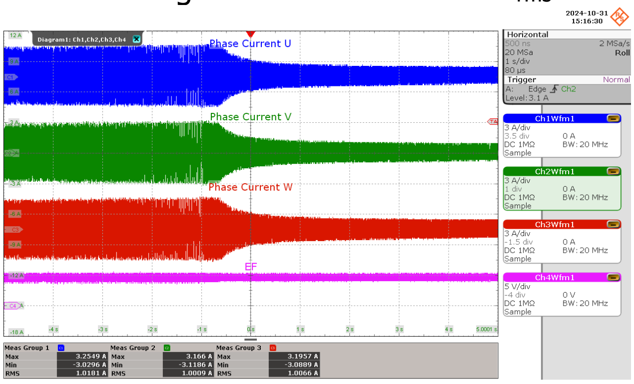

Figure 63 – Running Overload Test.
CH1: $I_{PHASE(U)}$, 3 A/div.
CH2: $I_{PHASE(V)}$, 3 A/div.
CH3: $I_{PHASE(W)}$, 3 A/div.
CH4: V_{EF}, 5 V/div.
Time Scale: 1 s/div.

8 Appendix

8.1 Board Quick Reference

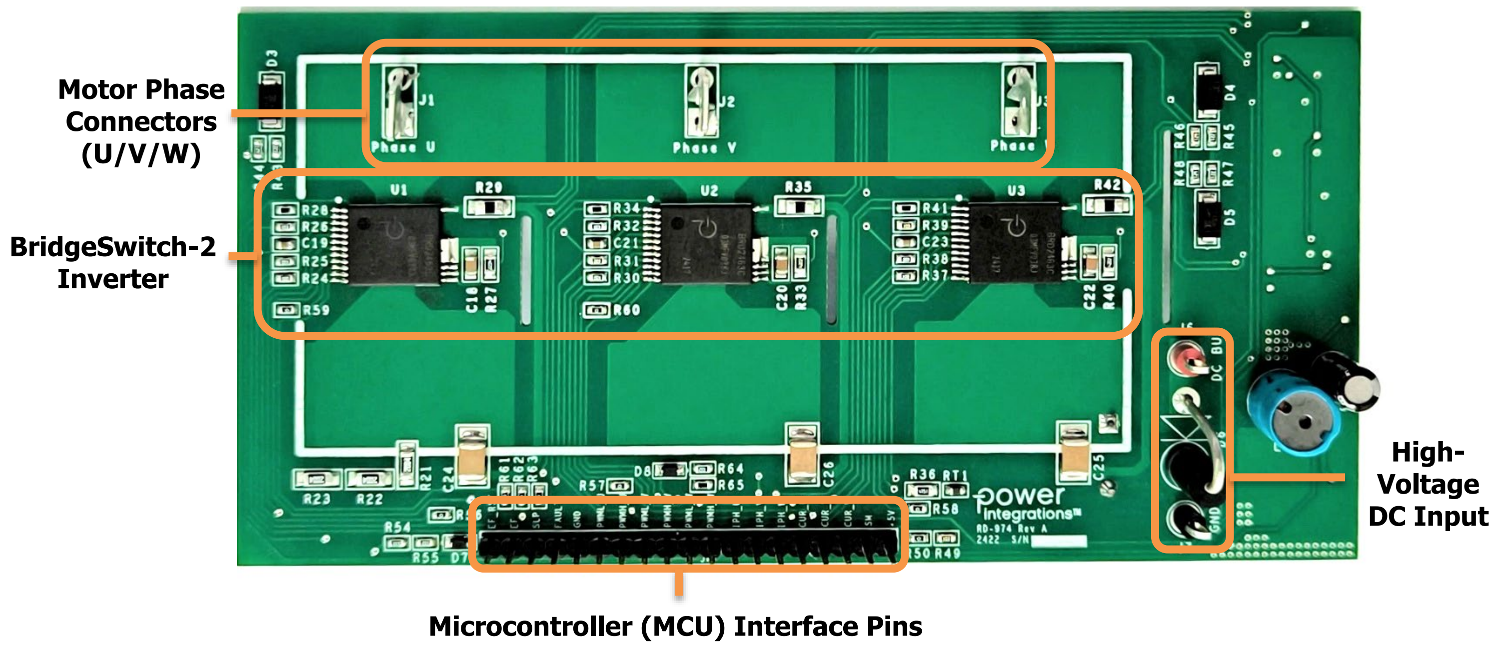

Figure 64 – RDK-974 Board Quick Reference.

8.1.1 Microcontroller (MCU) Interface Signals

- **EF_RST** – Error flag reset signal interface
- **EF** – Pin for error flag state monitoring and inhibiting FREDFET switching
- **SLP** – Sleep mode control signal interface
- **GND** – Common ground interface between the microcontroller and the inverter board
- **PWMH_U, PWML_U, PWMH_V, PWML_V, PWMH_W, and PWML_W** – PWM input signal interface
- **+5 V** – Voltage supply pin for the microcontroller as needed
- **SM** – Configurable system monitoring pin for the BridgeSwitch device (U2)
- **Curr_fdbkU, Curr_fdbkV, Curr_fdbkW** – Current feedback information from the shunt resistors processed by the signal conditioning circuit
- **IPH_U, IPH_V, IPH_W** – Low-side power FREDFET instantaneous phase current information from each BridgeSwitch-2 device

8.1.2 J4 Connector Pin Designation

Pin No.	Signal	Type	Comments
1	+5 V	Output	Voltage supply pin for the microcontroller as needed.
2	SM	Input	External input for system monitoring components.
3	Curr_fdbkW	Output	Current feedback information from the signal conditioning circuit for phase W.
4	Curr_fdbkV	Output	Current feedback information from the signal conditioning circuit for phase V.
5	Curr_fdbkU	Output	Current feedback information from the signal conditioning circuit for phase U.
6	IPH_W	Output	Voltage signal proportional to the instantaneous phase W low-side FREDFET Drain current.
7	IPH_V	Output	Voltage signal proportional to the instantaneous phase V low-side FREDFET Drain current.
8	IPH_U	Output	Voltage signal proportional to the instantaneous phase U low-side FREDFET Drain current.
9	PWMH_W	Input	Gate drive signal for the phase W high-side power FREDFET.
10	PWML_W	Input	Gate drive signal for the phase W low-side power FREDFET.
11	PWMH_V	Input	Gate drive signal for the phase V high-side power FREDFET.
12	PWML_V	Input	Gate drive signal for the phase V low-side power FREDFET.
13	PWMH_U	Input	Gate drive signal for the phase U high-side power FREDFET.
14	PWML_U	Input	Gate drive signal for the phase U low-side power FREDFET.
15	GND	N/A	Ground reference for the connector input and output signals.
16	FAULT_BUS	Input/Output	Single-wire, bidirectional fault communication bus.
17	SLP	Input	Sleep mode control signal.
18	EF	Output	Error flag state.
19	EF_RST	Input	Error flag reset signal.

Table 7 – J4 Connector Pin Designation

Note: The connections are labeled accordingly on the reference design board.

8.2 Recommended Start-up Sequence

BridgeSwitch-2 devices support PWM switching frequencies up to 20 kHz in self-supply mode. To ensure sufficient supply voltage levels across the BPL and BPH pin capacitors at inverter start-up, the system microcontroller (MCU) should follow the recommended power-up sequence depicted below.

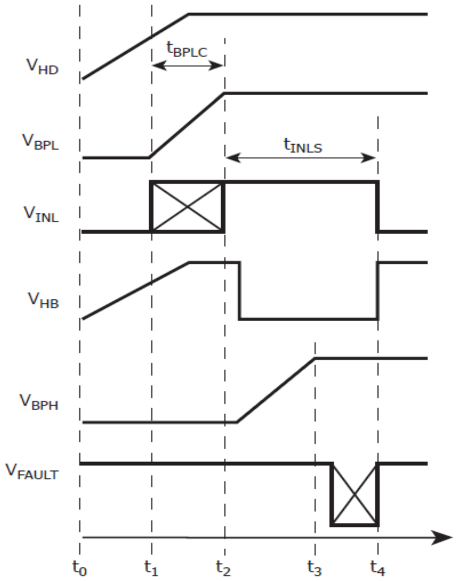

Figure 65 – Recommended Power-up Sequence with Self-Supplied Operation.

The table below describes each part of the recommended power-up sequence.

Time Point	Activity
t_0	• A high-voltage DC bus is applied
t_1	• The internal current source starts charging the BPL pin capacitor once the HD pin voltage reaches $V_{HD(START)}$ • The system MCU may start setting the low-side power FREDFET control signal INL to high
t_2	• The BPL pin voltage reaches V_{BPL} (typ. 12.8 V) • The device determines external device settings • The internal Gate drive logic turns on the low-side power FREDFET after device setup completes and once INL becomes high or if it is already high • The internal current source charges the BPH pin capacitor
t_3	• The BPH pin voltage reaches V_{BPH} with respect to the HB pin (typ. 12.8 V) • The device starts communicating successful power-up through the fault pin (for BRD216x and BRD226x only) Note: The device does not send a status update if the internal power-up sequence did not complete successfully.
t_4	• The BridgeSwitch-2 device is ready for state operation • The system MCU turns off the low-side power FREDFET

Table 8 – Power-up Sequence with Self-Supplied Operation.

8.3 Inverter Output Power Measurement

The inverter output power (P_{OUT}) can be measured using the setup in Figure 66 due to the availability of a six-channel power analyzer (WT1806E). This allows phase current readings for all three motor phases. Unlike the typical three-wattmeter implementation, a false neutral node was not created for the voltmeter connections, resulting in an identical total output power calculation as the two-wattmeter setup.

$$P_{OUT} = P_{CH1} + P_{CH2}$$

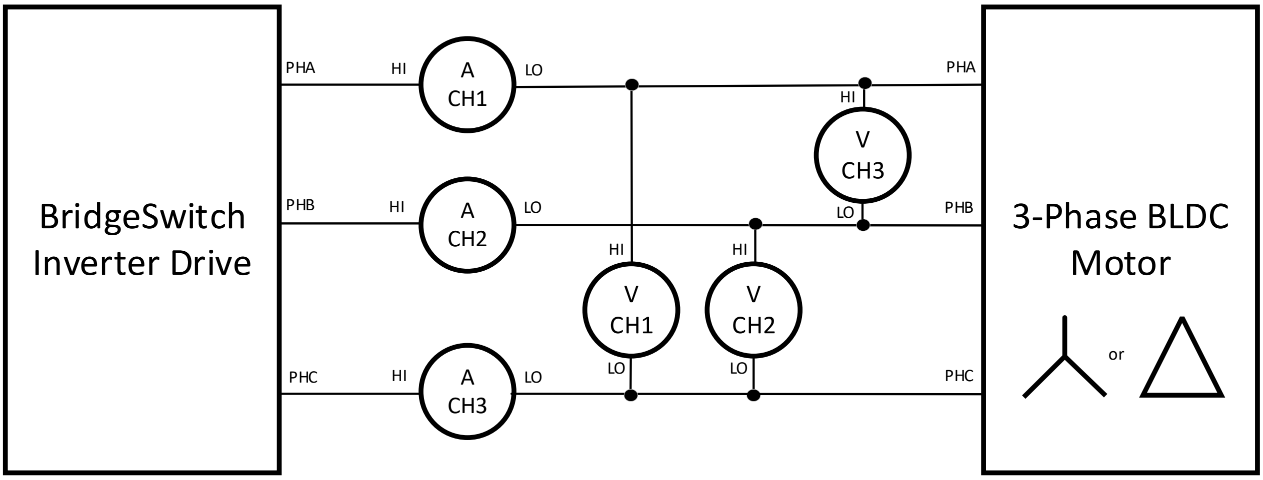

Figure 66 – Inverter Output Power Measurement (Three-wattmeter Setup).

Alternatively, the two-wattmeter setup in Figure 67 may be used to simplify connections and lessen the power meter quantity requirement. This yields similar readings to the three-wattmeter method previously described.

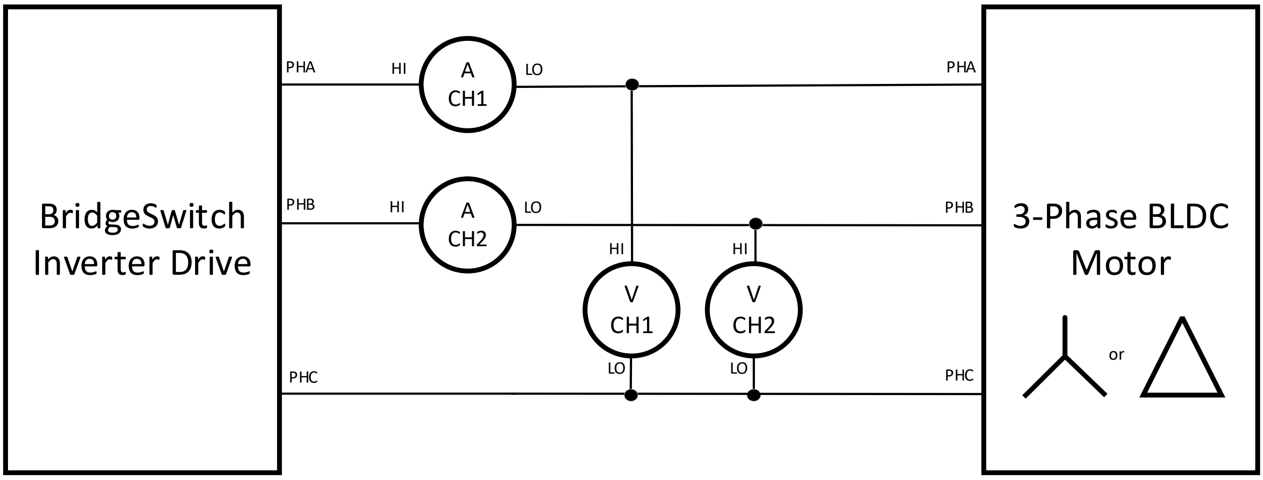

Figure 67 – Inverter Output Power Measurement (Two-wattmeter Setup).

8.4 No-Load Input Power Measurement

The no-load input power is recorded using the setup in Figure 68. A digital multimeter set to measure DC current in the micro-ampere (μA) range is recommended due to the lower range limitations of the power meter. This results in lower current readings than the power meter at its lowest current range (10 mA).

For the bus voltage, the power meter provides accurate measurements as its level falls within the available voltage ranges. The input power is computed using the formula below:

$$P_{IN} = V_{IN} \times I_{IN}$$

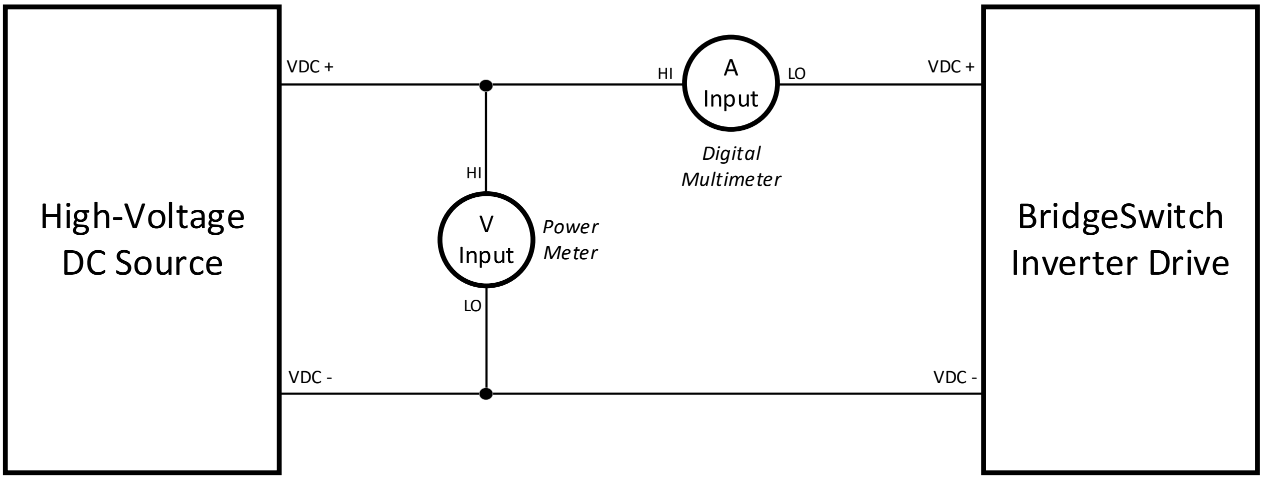

Figure 68 – No Load Input Power Measurement Setup.

8.5 IPH Reconstruction by the MotorXpert Suite

The instantaneous phase current (IPH) output of the BridgeSwitch-2 device is a low-voltage signal proportional to the positive phase current through the low-side power FREDFET. For use in field-oriented control, a reconstruction algorithm is required to derive the negative half-cycle current information.

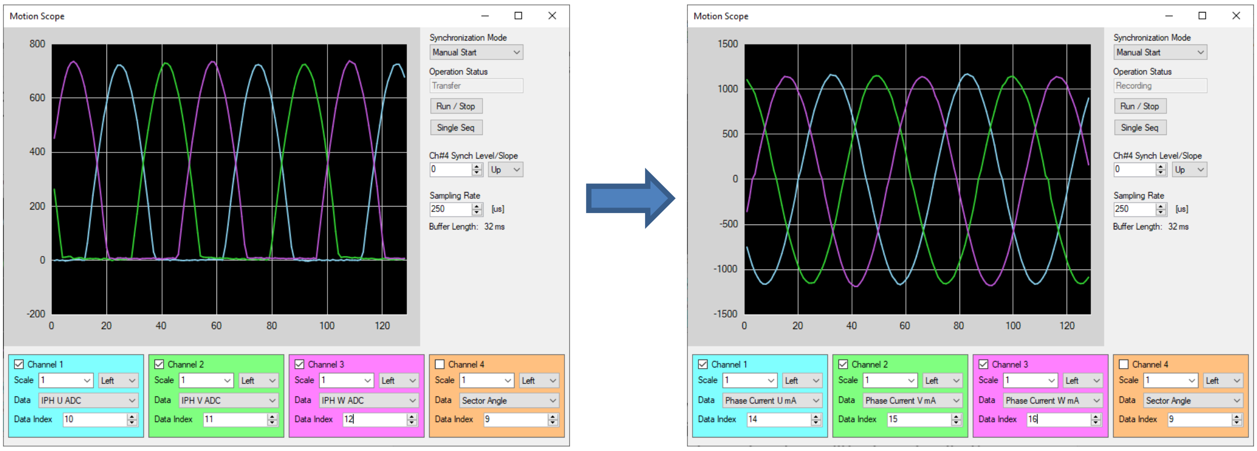

Figure 69 – IPH Signals after Phase Current Reconstruction.

The IPH signal reconstruction results in Figure 69 is created through the MotorXpert Suite by utilizing the known phase current signals trigonometric relationships. Unlike the current information from shunt resistors, the reconstructed signal maximizes both the positive and negative data ranges, resulting in twice the data resolution and enhanced current control.

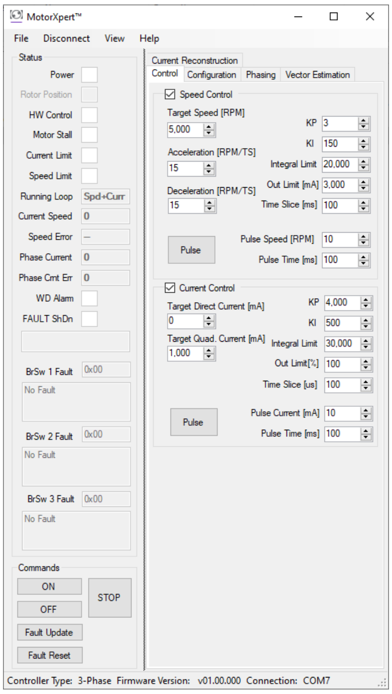

Figure 70 – MotorXpert Suite Window.

For more information about the MotorXpert Suite, visit the link below:
https://www.power.com/design-support/motorxpert-suite-bridgeswitch

8.6 FAULT and Error Flag Configurations

This reference design is compatible with both FAULT (BRD226x) and Error Flag (BRD246x) BridgeSwitch-2 variants. The Error Flag (EF) offers a simpler fault flagging scheme compared to the FAULT bus, but only for destructive faults. Shown in Table 9 are the operating conditions flagged by each one.

FAULT Conditions	Error Flag (Default)	FAULT
HV Bus OV	✓	✓
HV Bus UV (100%, 85%, 70%, 55%)		✓
System Thermal Fault		✓
LS Driver Not Ready		✓
LS FET Thermal Warning		✓
LS Device Shutdown (OTP, Latching OCP)	✓	✓
HS Driver Not Ready		✓
LS FET Cycle-by-cycle Overcurrent		✓
HS FET Cycle-by-cycle Overcurrent		✓
LS FET Latching Overcurrent	✓	✓
Device Ready (No Faults)		✓

Table 9 – Error Flag and FAULT Bus Triggers.

To isolate either functionality, shorting resistors (0 Ω) are incorporated into the design. Summarized in Table 10 is the component configuration requirements for the Error Flag and FAULT bus.

Component Description	Error Flag (Default)	FAULT
BridgeSwitch-2 Device	U1, U2, U3 (BRD236x/BRD246x)	U1, U2, U3 (BD216x/BRD226x)
Pull-up Resistor	R54 (43 kΩ)	R49 (10 kΩ)
Shorting Resistors (Bus)	R61, R62, R63 (0 Ω)	R56, R57, R58 (0 Ω)
Shorting Resistors (Device ID)	N/A	R59, R60 (0 Ω)
Microcontroller Interface Pin	J4 Pin 18 (EF), J4 Pin 19 (EF_RST)	J4 Pin 16 (FAULT_BUS)
Additional Components (EF Reset)	R55, D7 (3.3 kΩ, 1N4148WS)	N/A
Optional Components (System Monitoring)	N/A	RT1, R36, R50 (100 kΩ NTC, 4.75 kΩ, 0 Ω)

Table 10 – Error Flag and FAULT Component Configurations.

Note: The SM component values for the FAULT variant may be adjusted based on the desired system monitoring temperature threshold.

8.7 Test Bench Set-up

The setup in Figure 71 ensures the accuracy of temperature and efficiency measurements for the unit under test (RDK-974). The acrylic case minimizes air flow to prevent its effects on the performance data.

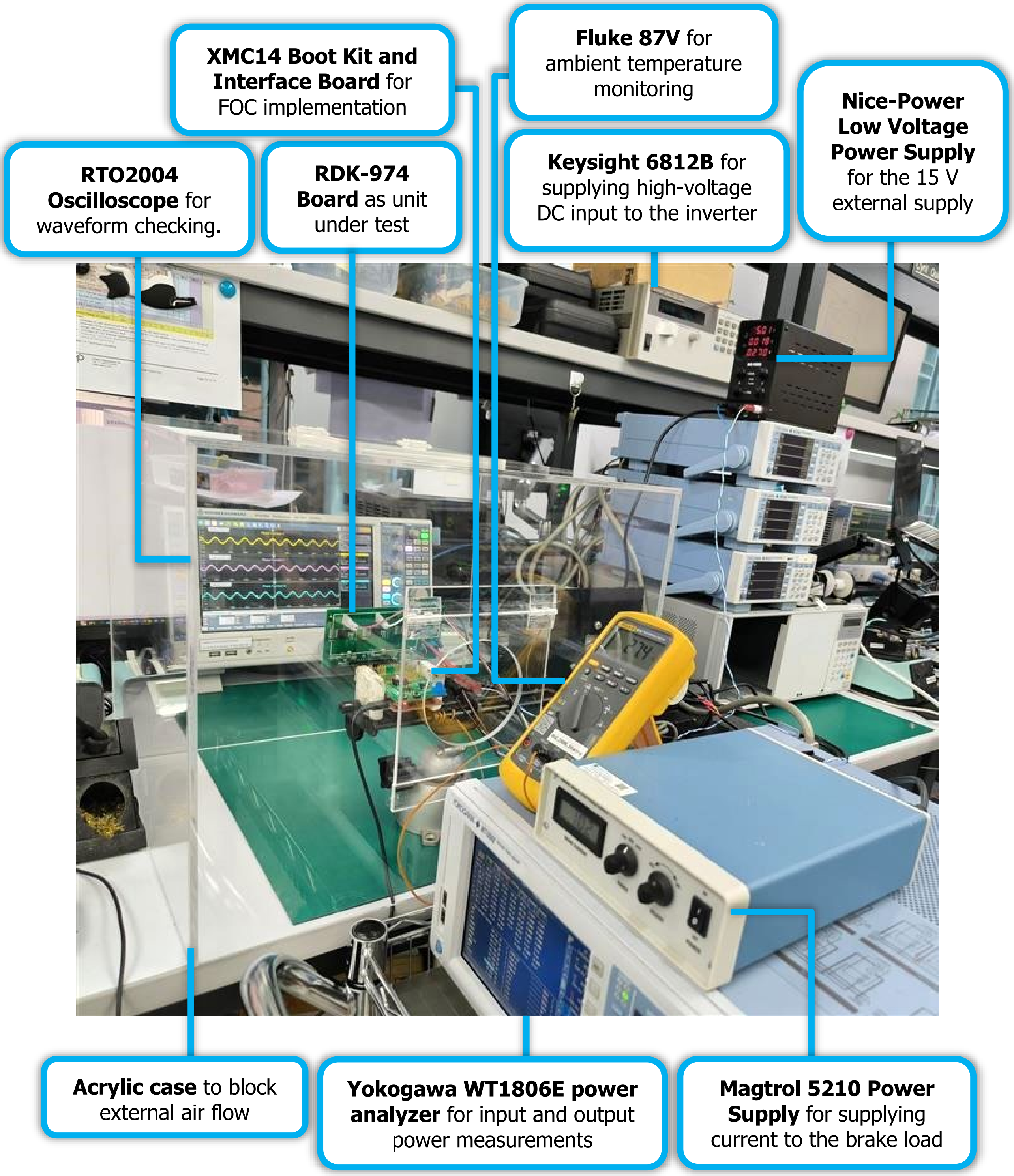

Figure 71 – Bench Set-up (Orthogonal View).

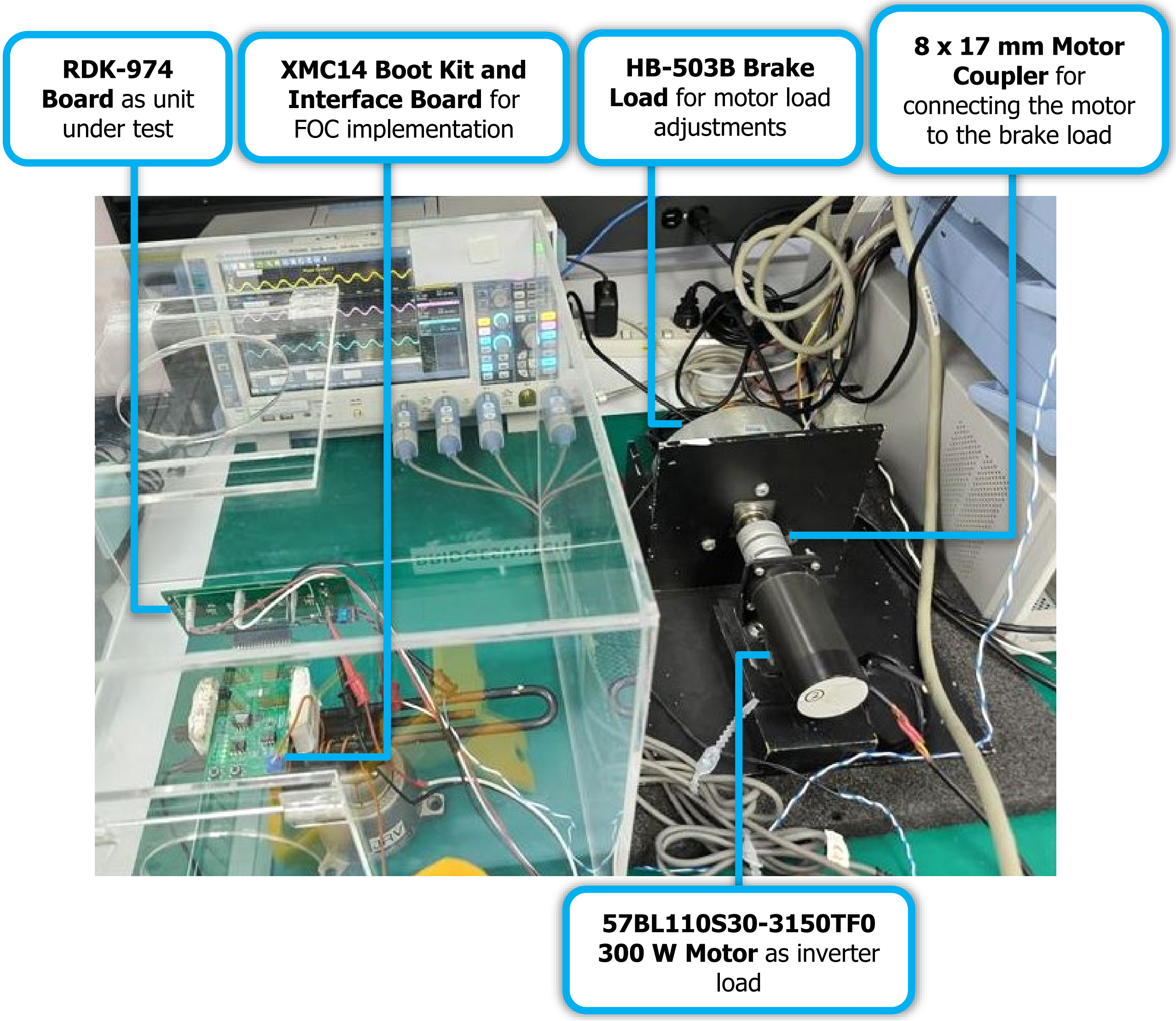

Figure 72 – Bench Set-up (Top View).

8.7.1 Equipment Used

1. **Motor (57BL110S30-3150TF0)** – 310 VDC, 300 W, 5000 RPM rated
2. **Motor brake load (HB-503B)** – 24 VDC, 300 W rated
3. **Brake load controller (Magtrol 5210)** – 24 VDC, 0 to 1000 mA output
4. **Motor Coupler** – 8 mm x 17 mm
5. **High-voltage DC Source (Keysight 6812B)** – 750 VA, 300 Vrms, 6.5 A rated
6. **Low-voltage DC source (Nice-Power)** – 30 VDC, 5 A maximum output
7. **Oscilloscope (RTO 2004)** – 600 MHz, 10 Ga/s resolution
8. **Digital Multimeter (Fluke 87V)** – -40 °C to 260 °C temperature range
9. **Precision Power Analyzer (WT1806E)** – 6-channel, 2 MS/s (16 bits), 0.1 Hz to 1 MHz measurement bandwidth

9 Revision History

Date	Author	Rev.	Description & Changes	Approval
31-May-24	SM	A	Initial Release.	Apps & Mktg
13-Sep-24	SM	B	Connectors J4 and J5 Merged. R54 Value, Significant Figures, and Minor Write-up Adjustments.	Apps & Mktg
19-Nov-24	SM	C	Added Abnormal Motor Operation Test.	Apps & Mktg

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