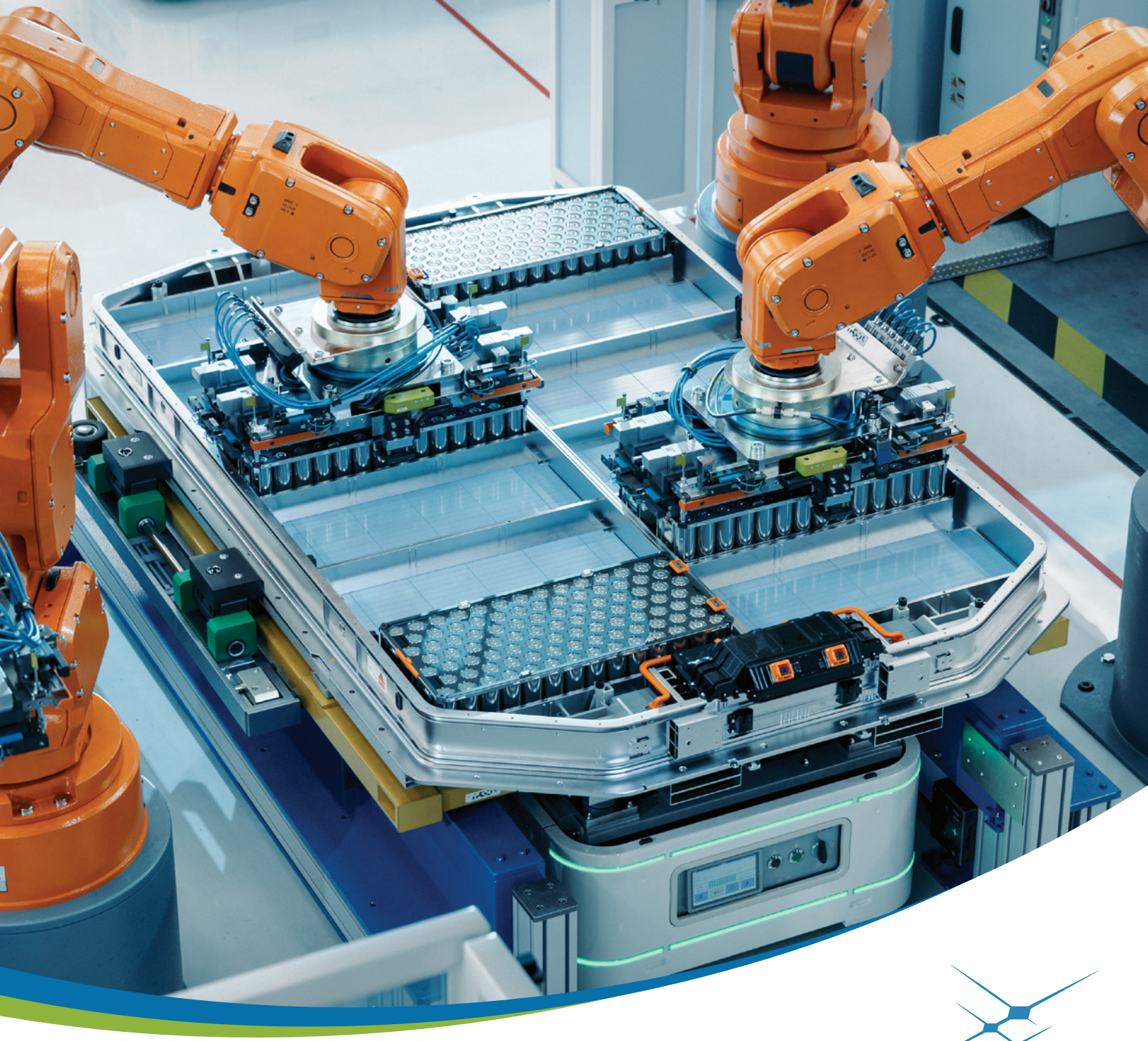

SKYWORKS®

SelVCD™: A Revolutionary Way of Driving Power MOSFETS in Gate Driver Applications

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As the global economy progresses along the paths of electrification and automation, the need for precise and reliable high-power electronics is growing. Reports suggest that the global market for power electronics for electric vehicles (EVs) alone will grow at a compound annual growth rate (CAGR) of 17% from 2025 to 2035 [1]. These, in addition to applications such as industrial robotics and renewables, are at the leading edge of electrification and automation. Yet, they are only as effective as their underlying power and control circuitry.

Gate drivers are fundamental and ubiquitous components in power electronics systems. But as demands for higher performance and efficiency mount, traditional gate drive architectures face significant shortcomings for use in next-generation applications.

Skyworks' SelVCD technology overcomes the limitations of traditional gate driver architectures to unlock unprecedented efficiency, performance, and reliability for power electronics applications.

A Background on Gate Drivers

Power electronics circuits are tasked with precisely controlling the movement of current throughout a system. Modern applications achieve this responsibility using three main components: Field-Effect Transistor (FET) power switches, isolated gate drivers, and microcontrollers (MCU).

A FET is an electronically controlled switch that enables or disables the flow of current through a system. The on/off switching behavior of a FET is determined by the timing and strength of a control signal applied to the device's gate. The FET turns on when the applied gate voltage exceeds a predetermined threshold voltage and turns off when the voltage falls below that threshold.

The FET's gate can be approximated as a capacitor, meaning that turning on the FET requires a build-up of charge until the accumulated voltage exceeds the device's threshold voltage level. Therefore, the characteristics of the applied gate-driving control signal significantly influence the performance and efficiency of the FET and the entire system.

An isolated gate driver is an electronic component designed explicitly to supply the switching current for charging/discharging a gate. The gate driver serves as a buffer between the low-level control electronics, which generally operate at 3 to 12V, and the higher-voltage power electronics, which generally operate at 60V and higher. This "level-shifting" behavior is necessary to provide suitable voltages to the transistor's gate without risking damage to the low-voltage subsystems. The MCU then acts as the brain of the operation, providing signals to control the gate driver's operation.

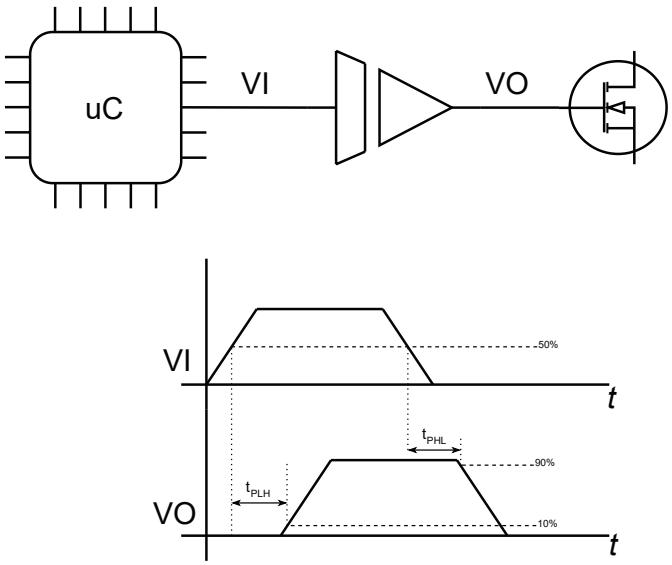

Figure 1: A simple architecture of an MCU sending gate driver signals to a power FET

In modern applications, designers need gate drivers that can provide high current drive, tightly control propagation delay, offer flexible packaging options, and are highly noise-immune.

Today, many gate drivers also include a galvanic isolation barrier, which provides the added benefit of protecting the controller from high voltages and transients, as well as maintaining noise-immune operation for optimal system efficiency.

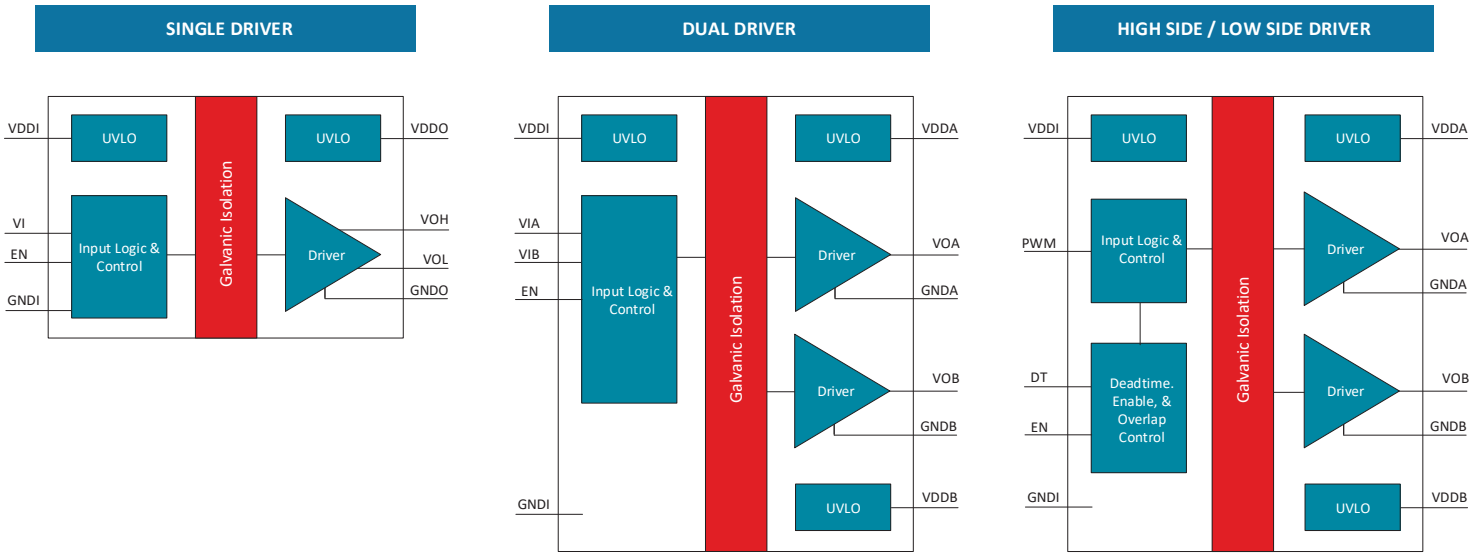

Figure 2: Some of the most common isolated gate driver configurations.

Applications for isolated gate drivers include:

- **Automotive:** on-board chargers, DC-DC converters, and traction inverters
- **Industrial and Motor Control:** uninterrupted power supplies and robot controllers
- **Infrastructure:** servers, cloud power, and solar inverters

Traditional Gate Drive Architectures

Most standard gate drivers operate as traditional voltage mode drivers (TVMD). These drivers function as a voltage source, delivering the necessary peak current to activate a FET by charging its gate input capacitor. They also offer a low-resistance discharge path to quickly turn off the FET. One important corollary of this control scheme is the need for additional components, namely resistors and diodes, between the gate driver and the gate itself (Figure 3).

Resistors are necessary between the driver and the gate to limit the peak current applied to the gate. A FET's gate can be modeled as a gate-to-source capacitor, and the current for charging this capacitor follows the conventional equation:

$$I_c = C\frac{dV_c}{dt} \qquad \text{(EQ1)}$$

where

I_c is the current charging the capacitor,

C is the capacitance of the capacitor, and

$\frac{dV_c}{dt}$ is the rate of change of voltage across the capacitor over time.

In accordance with EQ1, when a voltage is suddenly applied to a FET's gate, the current change is essentially instantaneous. Because the current is directly proportional to the rate of voltage change, a large instantaneous voltage change produces a massive spike in current. Such peak currents could damage the gate driver and the FET. Therefore, a TVMD requires a resistor situated between the gate driver and the gate to introduce impedance and limit peak currents.

The resistor in the TMVD is also necessary to control the gate driver's slew rate, which determines how quickly it can switch a transistor on or off by controlling the voltage at the gate terminal. In some cases, these systems can benefit from different resistor values depending on whether the switch is being turned on or off. Diodes are introduced to steer current through the appropriate resistor.

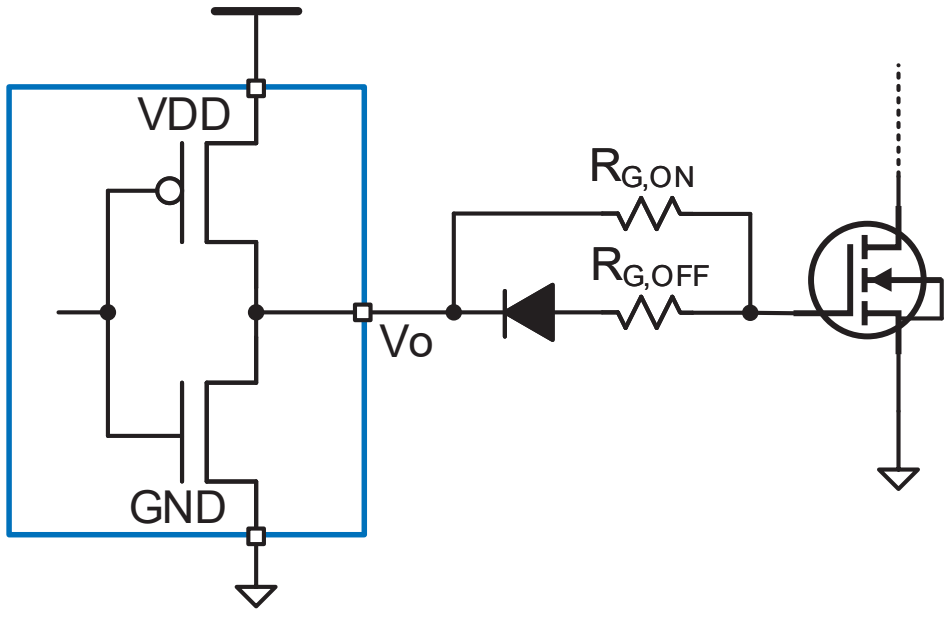

Figure 3: A traditional gate drive architecture, with the gate driver output stage modeled as an inverter.

Shortcomings of Traditional Architectures

While engineers have historically preferred a TVMD for their simplicity, the demands of modern power electronics have proven them to be a limiting factor in system design across a range of criteria, including performance and efficiency.

Limits in Efficiency

While the intentional addition of impedance is useful in limiting peak currents and controlling slew rates, the impedance introduces a significant source of power loss in the circuit. Specifically, power is burned through $I^2 R$ losses as current travels to the FET's gate during charging and discharging cycles. This power loss is significant, as designers must trade off between high resistor values to limit current spikes and low resistor values to improve switching speed. In EVs, for example, power losses associated with TVMDs can contribute to reductions in driving range.

Limits in Slew Rate

Gate resistors in gate drive circuitry are crucial for controlling the gate voltage slew rates. The size of these resistors determines how quickly a driven FET switches on and off. Using the smallest possible resistors allows more current to flow, charging or discharging a FET's intrinsic gate capacitor faster. However, this situation can lead to oscillations that may damage the gate over time.

To address the slew rate limitation, a larger driver can source and sink more current, along with carefully designing the gate resistors to prevent inductive gate ringing. A more sophisticated approach involves designing a gate driver with multiple outputs to enhance the sourcing and sinking current capability. Despite these methods, gate resistors are still necessary, and each approach introduces its own set of challenges.

A driver with multiple outputs increases the current needed to drive a gate, but determining the optimal number of outputs is complex. Moreover, a driver with multiple outputs does not guarantee the absence of gate voltage oscillations. Therefore, designing a gate driver with the precise number of outputs to achieve optimal switching efficiency while balancing voltage and current overshoots is both costly and intricate.

Lack of Flexibility

Power electronics applications like onboard chargers often operate in varying conditions that necessitate different gate drive behaviors. Different temperatures, for example, might require different drive currents or edge transition rates to optimize drive performance.

With resistive TVMDs, once designers choose resistor values for a given application, the values are fixed and cannot change. This lack of flexibility is an issue, as circuits thereby operate with the same gate drive behavior under all conditions. Ideally, gate drivers would be dynamic, optimally changing drive current and edge transition rates according to operating conditions.

Miller Effect in Half Bridge

In the typical scenario where a high-side/low-side (HS/LS) gate driver operates a half-bridge circuit connected to an 800 V bus, a common challenge for TVMDs is the Miller Effect (Figure 4).

The Miller effect is a phenomenon where the effective input capacitance of a MOSFET increases due to the feedback capacitance between the gate and the drain. This effect is significant because it impacts the switching speed and frequency response of the FET. In a half-bridge topology, the otherwise small intrinsic gate-to-drain capacitance can provide a parasitic path for current flow back from the drain to the gate.

Imagine a situation where the low-side FET in a half-bridge circuit is turned off, and the high-side FET is beginning to turn on. The parasitic Miller capacitance of the low-side FET can retain enough charge to create a rise in voltage at its gate. If this voltage surpasses the low-side FET's turn-on threshold voltage (usually around 2V), the FET will momentarily turn on, causing a significant current flow from the supply rail to ground, potentially damaging both the high-side and low-side FETs or at least causing a loss in switching efficiency.

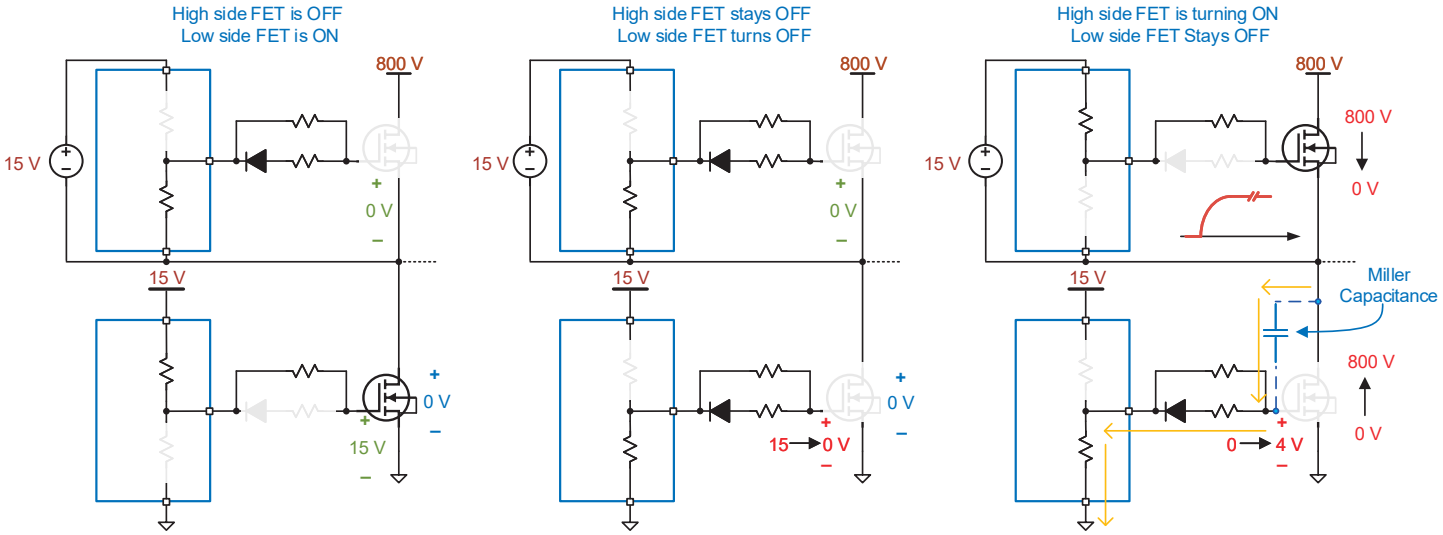

Figure 4: The impacts of the Miller Effect in a half-bridge being driven by an HS/LS driver.

The SelVCD Solution

Designers can address the challenges of resistive gate drives by choosing gate drivers with higher current sourcing and sinking capabilities. However, these higher current drivers do not resolve all the issues associated with TVMD. Additionally, they come at a higher cost and add complexity to the bill of materials. Skyworks has developed a superior solution with its Selectable Variable Current Drive (SelVCD) technology.

What is SelVCD?

SelVCD is a current-mode controlled gate drive solution capable of satisfying dynamic load demands. Unlike a TVMD, SelVCD drives transistor gates with a constant current and guarantees a precise ±10% current drive across process, voltage, and temperature variations.

Importantly, SelVCD features a programmable output constant current source controlled by a set of control pins on the device. With SelVCD, designers can adjust and optimize the gate voltage rise and fall slew rates and the output drive current, with eight independent drive strength selections for rising and falling edges.

And, since SelVCD is a current-mode device, it has the major benefit of not requiring any external resistors between the gate driver and the FET's gate (Figure 5).

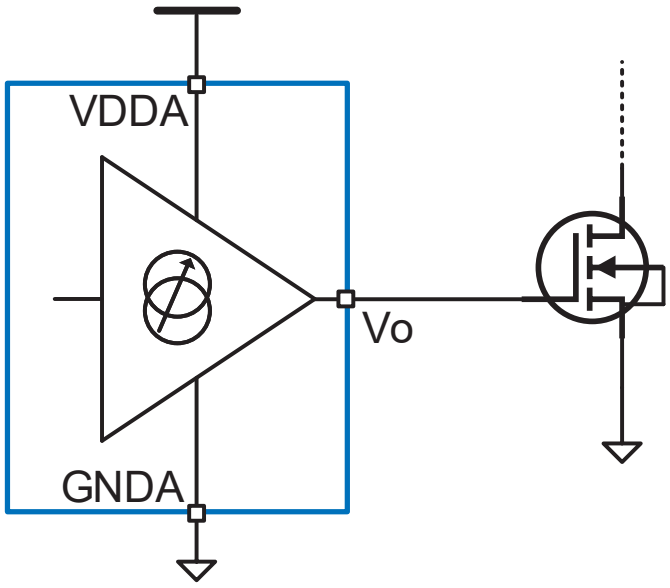

Figure 5: A gate drive topology using SelVCD eliminates the need for external resistors.

Better Efficiency

SelVCD addresses the power switching losses historically incurred by TVMD solutions. This advancement translates into improved efficiency as compared to a TVMD.

Slew Rate Control

SelVCD achieves precise control over gate voltage slew rates using its SPD+ and SPD− pins, which regulate the rising and falling edges, respectively.

The system offers eight distinct drive strength levels for each edge, ranging from SPD0 (the weakest drive) to SPD7 (the strongest drive). At SPD7, the drive strength reaches 100%, delivering the maximum slew rate, while at SPD0, the drive strength drops to 8.75%, providing a significantly slower slew rate. At the maximum setting (SPD7), the gate voltage transition can be completed in as little as 20 ns. Under lower SPD settings, transition times can extend beyond 100 ns.

This control allows designers to fine-tune the system for optimal switching characteristics. For example, in fast-switching applications such as high-frequency DC-DC converters, the higher SPD settings minimize switching losses by accelerating the gate charge process. Conversely, lower SPD settings slow down the transition to mitigate electromagnetic interference (EMI) and reduce gate ringing in situations requiring noise reduction, such as motor control systems.

Flexible Performance

Unlike TVMDs with fixed resistor values and operating behavior, SelVCD allows for the dynamic adjustment and optimization of slew rates and drive strengths as load conditions change.

For example, designers can implement a SelVCD circuit with closed-loop feedback that monitors conditions such as temperature, supply voltage fluctuations, and load current. By actively sensing these variables, the system can adjust the gate drive characteristics in real time, ensuring optimal switching performance. When the load current increases, SelVCD can boost the drive strength to reduce switching losses, while under lighter loads it can lower the drive current to minimize electromagnetic interference (EMI) and reduce overshoot or ringing.

Consider an EV, where power systems are exposed to harsh and varied operating conditions depending on factors such as weather, load variability, and temperature fluctuations. SelVCD's ability to monitor these variables and adapt performance accordingly unlocks a level of system control that would be impossible with a TVMD.

Built-in Miller Clamp

SelVCD drivers come equipped with a built-in Miller Clamp to help alleviate the impacts of the Miller Effect.

A Miller Clamp is a mechanism that provides a low-impedance path to the ground when the transistor is in the off-state (Figure 6). This path ensures that any voltage spikes or charge accumulations generated by the Miller capacitance during switching transients are safely diverted to ground, preventing the gate voltage from rising and unintentionally turning the transistor on.

Additionally, SelVCD without gate resistors is less susceptible to the Miller Effect. This is because the absence of resistive elements in the gate drive path allows faster charging and discharging of the gate capacitance, minimizing the voltage feedback between the gate and drain that amplifies the effective input capacitance.

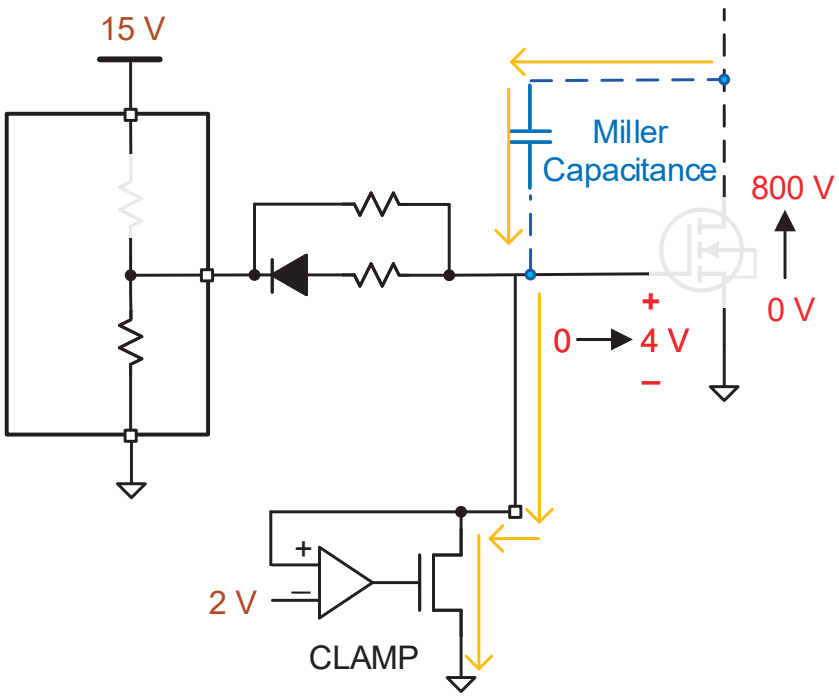

Figure 6: A Miller Clamp provides a path to ground to deliver unwanted currents away from a gate driver. This is an older approach. For SelVCD, the Miller clamp is fully implemented within the device.

Conclusions

As modern power applications require greater performance, efficiency, and reliability, conventional TVMDs are no longer the best option for gate drives. Instead, the current-mode gate drive enabled by SelVCD unlocks unprecedented efficiency, flexibility, and performance for next-generation applications.

SelVCD technology is currently available to customers in the new Si82Cx (single channel) and Si82Fx (dual channel) gate driver families from Skyworks. For example, our Si82Fx 2-channel High-Performance Isolated Gate Driver is the industry's first to feature the selectable variable current drive with a Miller clamp on both outputs. The Si82Cx is also the industry's first single channel gate driver to feature both SelVCD and a Miller clamp on the output pin.

To learn more about SelVCD, you can read this application note here: https://www.skyworksinc.com/-/media/SkyWorks/SL/documents/public/application-notes/AN1390-Dynamic-Speed-Control-of-the-Si82Fx-Performance-Driver.pdf

For more information about the Si82Cx and Si82Fx gate drivers, visit: https://www.skyworksinc.com/si82AFx

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